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Using UVM-ML library to enable reuse of TLM2.0 models in UVM test benches

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Abstract

As new IC process technologies are deployed, with decreasing geometrical dimensions, rapid progress is made in enabling integration of more and more transistors on a single chip. This makes it possible for hardware designers to implement more complex hardware architectures in their designs. Nowadays, a lot of the data processing algorithms are implemented in specialized HW instead of SW. The design flow usually starts with an early virtual prototypes development where reference models are developed to explore different aspects of the target algorithms, e.g. performance, accuracy and complexity.

The verification part of the ASIC development flow is also becoming ever more challenging and important as the design complexity increases. To address these challenges, ASIC verifiers can reuse the reference models in their self-checking verification environments together with their RTL designs to check the functional correctness of the algorithm implementation.

Both Loosely-Timed TLM 2.0 models as well as UVM test benches make use of sockets, ports, etc. and abstract data representation. By making the sockets/ports of both UVM and TLM/SystemC compatible, and being able to directly connect them, LT TLM 2.0 models become a natural fit to use with UVM test benches. The integration and connection of the TLM models into metric driven verification flow (UVM) can be accomplished by using UVM-ML library, which is a library that enables the communication between UVM-SV and TLM/SC (among other languages). Using an industrial case study, our work looks at the feasibility of using this approach.

In this paper, we provide a tutorial that answers practical UVM-ML integration and deployment questions and provides guidelines for adopting this technology. To demonstrate this in a full verification flow we developed an example that includes a RTL design, full UVM test bench, and TLM/SC reference model.

Keywords—UVM Multi Language; UVM-ML; UVM; SystemC; TLM; Metric Driven Verification, Code reuse, HW verification

I. INTRODUCTION

The ASIC verification tasks are getting more challenging and time consuming. Today, verification teams usually rely on reusing UVCs that are developed by different sources both inside and outside their organizations, e.g. from 3rd party vendors. When it comes to HW reference models, they also can be developed by different sources in different languages, on different abstraction levels, to fulfill different purposes. Each team selects the language, framework, and methodology that is most optimal for fulfilling their requirements. The hardware design flow usually starts with an early virtual prototypes development phase where reference models are developed to explore different aspects of the target algorithms, e.g. performance, accuracy and architecture complexity. These virtual prototypes are in some cases made available before the hardware design phase starts and are used as early software development platforms. To leverage all these different types of UVCs and HW reference models in verification testbenches users need to have a flexible and easy to use environment where these different components can co-exist and work seamlessly together.

Loosely-Timed TLM 2.0 reference models are a natural fit to use with UVM testbenches because both UVM, as well as TLM and SystemC®, make use of sockets, ports and abstract data representations, but they cannot be directly connected to each other which adds a limitation on the reusability of the reference models. To overcome the reusability limitation, verifiers need to manually implement an additional ad-hoc wrapper layer that enables the communication between TLM and UVM, e.g. by using DPI-C. A more generic solution is to use a library, like

UVM-ML, that enables direct communication between different frameworks. Other alternatives to using UVM-ML or using a manual ad-hoc solution based on DPI-C, is UVM Connect library [1], but this library doesn't support environments where users would like to extend the reusability scope to include other frameworks such as UVM-*e*.

Introduction to UVM-ML

UVM Multi-Language (ML) is an open-source library that enables the communication between UVM SystemVerilog (SV), SystemC/TLM, and Specman-*e*. Other languages/frameworks can be added as well. By using UVM-ML, verifiers can reuse the TLM models in their verification environments by directly connecting the ports of the UVM testbench to the ports of the TLM model. The UVM-ML library provides the solutions that enable the mixture and communication between different UVCs and HW reference models from different sources. Each component has its own requirements and therefore each language would have its own advantages and disadvantages. Using UVM-ML allows users to select the right language/framework/solution to solve the right problem and make the UVM-ML library abstract away each language/framework specific requirements.

The UVM Multi-Language library was originally developed in a collaboration between Cadence Design Systems and AMD. The people and the library were the base for the Accellera UVM-ML Open Architecture (OA) working group. The UVM-ML library is available as open source since 2012 at Accellera's community downloads [2] and it's also provided within Cadence® Xcelium™ installations.

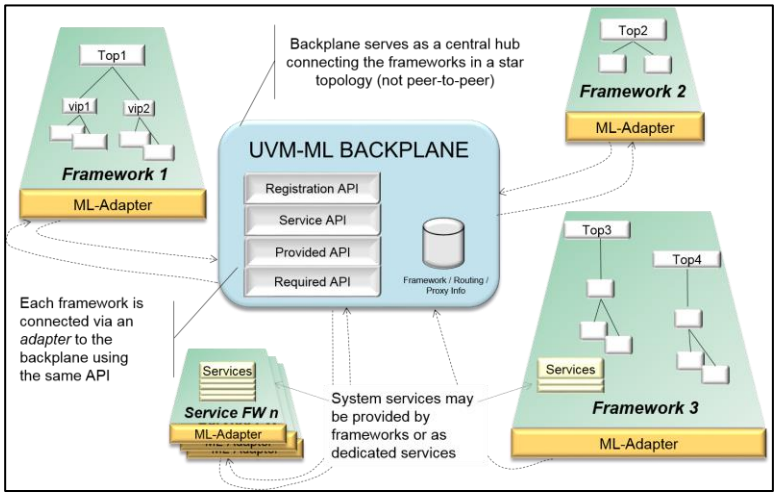

Figure 1: UVM-ML OA Architecture

In Figure 1, Framework 1 can be, for example, UVM SystemVerilog, Framework 2 – UVM-*e*, Framework 3-SystemC etc. The term framework denotes an assembly of verification and modeling facilities implemented in a single language. For example, a framework could be UVM SystemVerilog, UVM-*e*, SystemC etc. Different frameworks can be deployed in the same language (for example, UVM and OVM are both in SystemVerilog). A new framework can be composed from few simpler frameworks in the same language (for example, a combination of Accellera SystemC with a UVM SystemC library). The backplane serves as a hub between two or more integrated frameworks and holds information about the overall topology, which is necessary for routing. Each framework is connected via an adapter to the backplane using the same API. Any number of frameworks can be interconnected at the same time. The overall UVM-ML OA architecture enables collaboration between the frameworks while abstracting away from specific methodologies and languages. The backplane is also used for broadcasting messages from a service provider to the rest of the frameworks, for example the phasing service is implemented in this way.

UVM-ML OA Key Features include:

- Modular and extensible architecture: Users can add ML-Adapters to support additional frameworks such as OVM.
- Framework and simulator independent API.

- Supports TLM communication (both TLM 1.0 and TLM 2.0).
- Offers coordinated initialization/bring-up and phase synchronization of all participating libraries.
- Offers unified hierarchy solution:
  Hierarchical construction of a multi-language verification environment.
- Multi-language configuration: Configuration items are created in top framework and then propagated to other frameworks in the environment.
- Multi-language sequence layering.

Phase synchronization means coordinating phases between the various frameworks. It also ensures that components are *configured* then *created*, and ports are *created* then *connected*, etc. Figure 2 shows the order of phase execution when having 3 frameworks: UVM-SV, UVM-SC, and UVM-*e*.

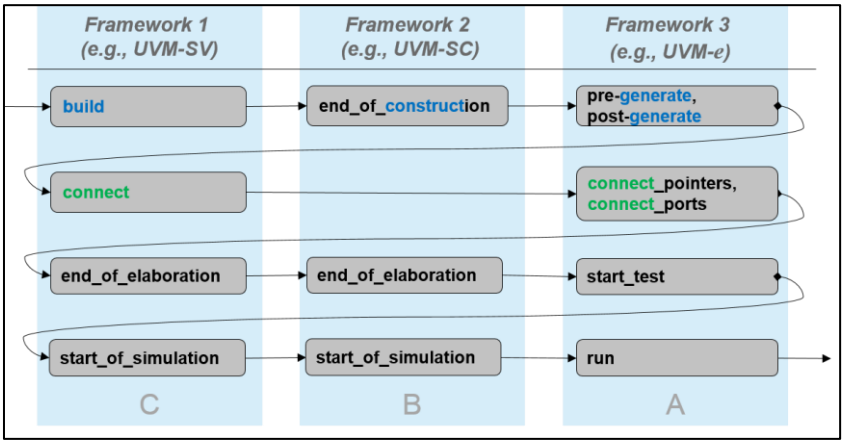

Figure 2: Phase synchronization between UVM-SV, UVM-SC, and UVM-e

Data communication across different frameworks is done by using TLM ports (both TLM 1.0 and TLM 2.0) including both blocking and non-blocking variants. In recent UVM-ML releases support for TLM analysis ports was also added. The data types that are transported across the different platforms are also converted and matched by the UVM-ML library. The requirement is that serialization and de-serialization routines are provided to the library, so it can pack/unpack struct and class in a consistent format that can be passed across the different frameworks. In most cases the UVM automatic field macros provide the necessary data packing/unpacking mechanism.

II. RELATED WORK

This work is based on the Accellera UVM Multi Language Open Architecture library [2]. The underlying technologies are UVM (Universal Verification Methodology) and TLM (Transaction-level Modeling) from Accellera working groups.

In this work, we will show the steps to integrate and use UVM-ML to enable the communication between UVM-SV and TLM/SC in a full verification flow to verify a RTL DUT. The presented example includes a simple RTL design, full UVM TB, and TLM/SC reference model. The test bench is implemented completely according to UVM methodology. All components are realized in order to demonstrate seamless UVM-ML integration. It captures a simple but realistic test case. The presented example also shows how to implement the test bench according to "unified hierarchy" approach. This allows users to instantiate a component, e.g. the TLM reference model, under a test bench of different type, such as UVM-SV, and present the full hierarchy as one test bench hierarchy. The alternative to using the unified hierarchy approach is using the traditional side-by-side approach where the TLM model is instantiated in a separate top in parallel with the UVM test bench hierarchy.

UVM-ML is widely adopted in industry projects to enable reuse of different verification environments implemented in different frameworks/languages and integrate them together. Many different groups inside or

outside an organization might select different verification languages to best address their challenges. Each language would have its own advantages and disadvantages for a given component and the focus for each group is on selecting the right language/framework to solve their specific challenges. This raises the need for a flexible platform that supports multiple verification languages working together to enable code reuse [3].

III. APPLICATION

In this work, we implemented a RTL DUT and a full UVM-SV verification environment [6]. Then we instantiated a LT TLM/SC reference model inside the test bench and used UVM-ML to connect the TLM sockets between SV and SC domains. By including the TLM model in the verification environment we are able to add a UVM scoreboard that compares the responses from the DUT against the responses from the TLM reference model. The goal was to achieve a self-checking test bench without having to re-model the DUT functionality/algorithm in the UVM environment.

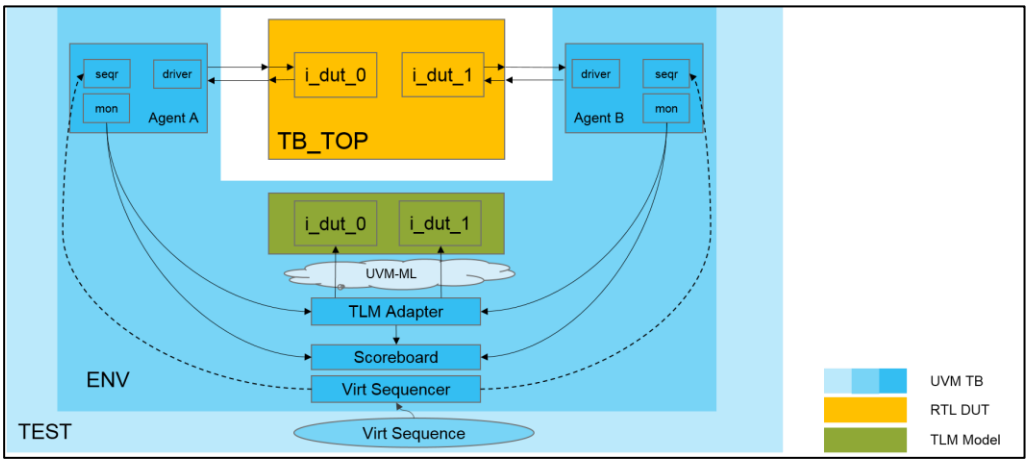

Figure 3: Topology of the example verification testbench

The TLM adapter receives UVM sequence items, from the UVC monitor, and maps them to TLM generic payloads *uvm_tlm_gp* (GP) and then sends them, over UVM-ML, to the TLM reference model. The *b_transport* function of the TLM model adds the expected data (including GP extensions) and responses to the GP and then returns. After the TLM transaction is done, the TLM model's response is passed back to the scoreboard through the TLM adapter. This way the scoreboard component can compare the functionality of the RTL DUT against the TLM reference model. The verification environment fully complies to UVM-SV 1.2 methodology and includes UVM-ML OA v.1.9. As per UVM methodology the UVC monitors offer functional coverage collection (covergroup) on sampled transactions, and the UVM test sequences use constraint-random data generation. The simulator used is the Cadence Design Systems Xcelium™ simulator. The test cases implemented in this case study send transactions to the DUT using an interface UVC according to UVM methodology.

In this TB the unified hierarchy approach was used where SystemC/TLM reference model was instantiated under a UVM-SV component. Each type must be defined in the respective language. In the UVM-SV component **Define** a member of type "**child_component_proxy"** (or "**uvm_component"**, which it inherits). Then **Create** it using "**child_component_proxy uvm_ml::uvm_ml_create_component()".** The arguments are: Target framework name that implements the foreign child component, foreign class type, instance name in SV domain, and the parent instantiating this component.

Example 1: Instantiation of UVM-SC component under UVM-SV

```
//UVM-SV code
class myenv extends uvm_env;
  uvm_component tlm_wrapper_inst;
 function void build_phase(uvm_phase phase);
  …
  tlm_wrapper_inst = uvm_ml_create_component(
                          "SC","top_wrapper","tlm_wrapper_inst",this);
  endfunction
  …
```

```
//UVM-SC code
class top_wrapper : public uvm_component {
  //Instantiate the TLM model here.
}
```

The DUT is a SystemVerilog RTL module that contains 32 x 32-bit wide general-purpose registers which can be accessed through a R/W bus interface. To demonstrate a more realistic DUT example that requires configure before use, 2 configuration registers were added to this design to control its behavior. By default, the general-purpose registers are not accessible for read or write access until a "block_enable" register is set. By setting this register the general-purpose registers will be accessible in read-only mode. To make the general-purpose registers accessible in read-write mode a "reg_write_enable" register needs to be set as well. The goal was to capture a simple but realistic use case example that demonstrates how to integrate the TLM model with a UVM-SV test bench by using the UVM-ML library. Similar test bench layouts are used in real life projects to verify designs found in communication, image processing, and HW control applications.

This approach enables HW verifiers to reuse TLM models in their verification environments to build more sophisticated test benches in a standardized, structured and reusable way. This methodology could be applied to both Simulation and Emulation/TBA (Transaction-Based Acceleration) based verification environments.

IV. UVM-ML INTEGRATION STEP BY STEP

Importing the UVM-ML Library

In addition to the RTL and testbench code, users need to include UVM-ML features by loading/compiling the backplane and adapters to be used. The SV adapter is a SV package "uvm_ml::*" and it needs to be imported after the UVM package and macros include to become part of the SV compilation. In SC this is included by using an include header file "uvm_ml.h". If TLM 2.0 is used, then "ml_tlm2.h" needs to be included as well.

Example 2: Importing the UVM-ML library in UVM-SV and UVM-SC

```
//UVM-SV code
import uvm_pkg::*;
`include "uvm_macros.svh"
import uvm_ml::*;
```

```
//SC code
#include "uvm_ml.h"
#include "ml_tlm2.h"
```

Running the Test Under UVM-ML

When incorporating UVM-ML in your environment, UVM-ML has to take control over building your UVM environment and running its phases. This is done by using the UVM-ML method "uvm_ml_run_test(string)" in the test bench top module instead of using the regular UVM "run_test()" method. The test name can still be passed using the plus argument +UVM_TESTNAME.

Example 3: Running the UVM environment under UVM-ML

```
//UVM-SV code
string tops[1];
initial begin
  …
  tops[0] = "";
  uvm_ml_run_test(tops);
end
```

Socket Registration on SV Side

Using UVM-ML APIs, UVM-SV sockets are registered for connection to SC domain. The registration should be done at *phases_ended()* of *build* phase using the "**register**" UVM-ML function.

Example 4: Registration of UVM-SV sockets in UVM-ML

```
//UVM-SV code
function void phase_ended(uvm_phase phase);
    if (phase.get_name() == "build") begin
            uvm_ml::ml_tlm2#()::register(initiator_socket_0);
            uvm_ml::ml_tlm2#()::register(initiator_socket_1);
    end
 endfunction
```

Socket Registration on SystemC Side

The sockets registration needs to be done in SystemC® side as well. This can be achieved by using the socket registration macros. The socket registration macros return a string value, which is the hierarchical path to the socket after elaboration. This can be printed out for debugging.

Example 5: Registration of UVM-SC sockets in UVM-ML using socket registration macros

```
//UVM-SC code
void build() {
   full_target_socket_name_0 = ML_TLM2_REGISTER_TARGET(dut_inst, tlm_generic_payload, reg_in_0, 32);
   full_target_socket_name_1 = ML_TLM2_REGISTER_TARGET(dut_inst, tlm_generic_payload, reg_in_1, 32);
}
```

Instead of using the macros, you can also call the socket registration functions (*ml_tlm2_register_initiator* and *ml_tlm2_register_target*) directly in order to take advantage of all additional arguments provided [4,5].

Example 6: Registration of UVM-SC sockets in UVM-ML using socket registration functions

```
//UVM-SC code
#include <sstream>
ml_tlm2_register_initiator <tlm_generic_payload, 32>(*inst, inst->o_port[0], "o_port_0");
for(int i = 0; i < 16; i++) {
   std::ostringstream osstr; osstr << i;
   ml_tlm2_register_target<tlm_generic_payload, 64>(*inst, inst->i_port[i], "i_port_"+ osstr.str());
}
```

Socket Connection

After registering the sockets on both SV and SC sides with UVM-ML, the next step is to connect these sockets. The connection from SV to SystemC® domain can be done in either the SV or SystemC® side. The following SV example code shows the connection inside the *connect_phase()* function using the UVM-ML "**connect**" function.

Example 7: Socket connection between UVM-SV and UVM-SC

```
//UVM-SV code
function void connect_phase(uvm_phase phase);
    void'(uvm_ml::connect(initiator_socket_0.get_full_name(),
                          "uvm_test_top.tb_env.tlm_wrapper_inst.dut_inst.reg_in_0"));
    void'(uvm_ml::connect(initiator_socket_1.get_full_name(),
                          "uvm_test_top.tb_env.tlm_wrapper_inst.dut_inst.reg_in_1"));
endfunction
```

The SystemC sockets hierarchal path names (second argument to "connect" function) could be extracted either by looking into the topology of the testbench or using the return value of SystemC socket registration macros.

V. USING TLM GENERIC PAYLOAD EXTENSIONS WITH UVM-ML

On SystemVerilog side, the class that defines the GP extension fields must use the UVM field registration macros which define the packer and unpacker functions under-the-hood; these functions are used by UVM-ML library for serialization and de-serialization of GP for transporting and collecting data.

Example 8: Field registration macros on UVM-SV side

```
//UVM-SV code
`uvm_object_utils_begin(vip_transfer_gp_ext)
   `uvm_field_int(m_id, UVM_ALL_ON)
`uvm_object_utils_end
```

The field registration macros are needed in SystemC® side too; on the SystemC side, they are out-of-class macros. This enables code reuse as these macros can be added in a top TB file only when used in a TB that needs to send this class type across different frameworks.

Example 9: Field registration macros on UVM-SC side

```
//SC code
 ML_TLM2_GP_EXT_BEGIN(transfer_gp_ext)
    ML_TLM2_FIELD_ACCESSORS(uint32_t, get_id, set_id)
 ML_TLM2_GP_EXT_END(transfer_gp_ext)
```

In example 9 the "ACCESSORS" macro is used which uses the *get_id()*/*set_id()* member functions of the GP extension class to access the data field. This is because the data members are declared *private*; if they were *public* then we could use the macro "ML_TLM2_FIELD" that takes the data member itself as argument. Additionally, the order of the field registration macros should match in both SV and SystemC® sides for the data to be unpacked properly.

For UVM-ML to be able to convert and transfer data class objects between different frameworks, it needs to match the equivalent class names in each framework. The names of the GP extension classes in SystemVerilog and SystemC® side should match too; if they don't, matches need to be specified explicitly using the **set_type_match()** function.

Example 10: Manual type matching between SV and SC classes

```
//UVM-SV code
if(!uvm_ml::set_type_match("sv:vip_transfer_gp_ext","sc:transfer_gp_ext"))
   `uvm_fatal(get_name(), "Cannot match the GP extension types.")
```

In example 10 above the function call tells UVM-ML that the SystemVerilog class "vip_transfer_gp_ext", which is the class that specifies the GP extension, should be considered the corresponding match for the SystemC class "transfer_gp_ext".

Using the GP extensions is done as per regular TLM flow; no UVM-ML specific APIs are required. In both UVM-SV and SystemC®, use the ***set_extension()*** and ***get_extension()*** functions to add/get the GP-extension object to/from the GP object.

VI. UVM-ML INTEGRATION DEBUGGING HELPERS

The following points list few useful debugging features that could be used to debug any integration issues while incorporating UVM-ML in the verification environment.

1. You can add the following function call in your SC code, before any socket registration, to get the list of registered sockets in both SystemC and SV:
   void(uvm_ml_execute_command("uvm_ml_trace_register -on"));
2. You can also get the list of registered sockets by using this Xcelium™ TCL command:
   uvm_ml trace_register_tlm

3. To stop the simulation at the end of the connect phase and print the connections to make sure they've been done properly, use the following Xcelium™ TCL commands:
   uvm_ml_phase -stop_at -end connect
   run
   uvm_ml_print_connections

4. The following Xcelium™ TCL command shows the types being matched between the different frameworks:
   uvm_ml print_type_match

VII. RESULTS

By using UVM-ML library we were able to achieve a test bench architecture where the TLM reference model was instantiated as a component inside the verification environment. The complexity of the UVM scoreboard component was significantly lower as we didn't need to re-model the intended DUT functionality to support the self-checking test bench approach, and this allowed us to save TB development time by leveraging on code reuse. The reduction of the test bench complexity did not cause any decrease in verification quality. In real life projects it has been noticed several times that re-using HW reference models developed by a different team would actually improve the verification quality because it would reveal any mismatching assumptions concerning the DUT intended functionality that could be found due to e.g. ambiguous documentation.

Using UVM-ML for enabling reuse of TLM reference models in verification test benches is a proven solution that is applied by several users/companies. The example TB developed in this work shows that reusing TLM reference models in verification test benches, instead of reimplementing the same functionality, shortens the HW verification lead time and increases the verification quality/confidence.

The features offered by UVM-ML under the hood, such as unified hierarchy support and phase synchronizing between the various frameworks makes it easier achieve the desired TLM model reuse with minimal integration effort. In our work we also implemented a version of the test bench that uses DPI-C calls, instead of using UVM-ML library, to communicate between UVM-SV and SystemC domains. This allowed us to measure any simulation time overhead and compare the code complexity.

Using UVM-ML resulted in higher memory usage compared to the DPI-C TB implementation. The overall memory used in UVM-ML simulation was 167 MB compared to 146 MB in the DPI-C version of the test bench. Simulation time was slightly higher in the UVM-ML version as well, the average simulation time (net CPU time) for the UVM-ML version was 0.6 s compared to 0.4 s in the DPI-C version.

On the other hand, the code complexity was higher in the DPI-C version. DPI can handle conversion of basic data types between SystemVerilog and SystemC but, unlike UVM-ML, it cannot handle auto conversion of class objects. The DPI-C function that is called from SV side had to collect the transaction attributes and place them inside a TLM GP before sending them over the sockets. The DPI-C function had to be implemented in the global SC scope. To be able to access the sockets of the TLM reference model from inside this global function, additional ad-hoc code was added to get the correct *sc_module* object and drive the transaction on its sockets.

Example 11: DPI-C function that is called from SV side to send transactions on SC side.

```
extern "C" bool write_rtl2tlm(bool &index, int &data, int &addr, bool &wnr) {
 //put transaction attributes in a TLM GP
 tlm::tlm_generic_payload * trans = new tlm::tlm_generic_payload();
 trans->set_command((wnr ? tlm::TLM_WRITE_COMMAND:tlm::TLM_READ_COMMAND));
 trans->set_address(addr);
 trans->set_data_length(4);
 trans->set_data_ptr(reinterpret_cast<unsigned char*>(&data));
 trans->set_streaming_width(4);
 trans->set_response_status(tlm::TLM_INCOMPLETE_RESPONSE);
 sc_time delay = SC_ZERO_TIME;
```

* Cadence Design Systems, Inc.

```
//Prepare a GP extension and attach it to the GP
 transfer_gp_ext * gp_ext = new transfer_gp_ext();
 gp_ext->set_id(index);
 trans->set_extension(gp_ext);
//Get the pointer to the TLM module that implements the sockets
 dut_wrapper * i = (dut_wrapper*) sc_find_object("dut_wrapper_inst");
 sc_assert(i);
//Send the transaction
 i->reg_out->b_transport(*trans, delay);
//take back results from GP -> ref args
 wnr = (trans->get_command()==tlm::TLM_WRITE_COMMAND ? 1:0);
 addr = trans->get_address();
 trans->get_extension(gp_ext);
 index = gp_ext->get_id();
 unsigned int len = trans->get_data_length();
 memcpy(trans->get_data_ptr(), &data, len);
 if ( trans->is_response_error() )
  return 0;
 else
  return 1;
}
```

The TLM model had to be edited as well to make it give this specific DPI-C function access to its private members by making it a "**friend**" of this class.

Example 12: Modification needed to TLM model to allow the global DPI-C function to access its internal sockets

```
//SC code
SC_MODULE(dut_wrapper) {
   …
   friend bool ::write_rtl2tlm(bool &index, int &data, int &addr, bool &wnr);
   …
};
```

The debug features offered by UVM-ML made it possible to list registered sockets and connections between the different frameworks, which is not available when not using UVM-ML. Other advanced features like phase synchronization and Multi-language configuration across different frameworks are also not available when not using UVM-ML.

VIII. CONCLUSIONS

Using UVM-ML is easy and straight forward. The UVM-ML library has been made available for few years and it's stable and well documented. The benefits of reusing TLM models in HW verification are: increased verification quality, lower test bench development time, and ascending the RTL verification scope to include HDL algorithm implementation and higher-level system functionality.

UVM-ML has been widely adopted across the ASIC industry to address real life problems and challenges. It becomes most valuable when companies have HW reference models or UVCs that could be reused in the verification space to increase quality and reduce TB development efforts. UVM-ML also gives users the opportunity to reuse different verification environments implemented in different frameworks/languages and integrate them together.

So, to reduce the verification time/effort, without sacrificing quality, users should reuse reference models if they are made available by other teams. The integration of these reference models with the verification environments is easily achievable by using UVM-ML library.

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