Fault Effect Propagation using Verilog-A for Analog Test Coverage

Aishwarya Prabhakaran

Ahmed Sokar

Jaafar Mejri

Agenda

1. Analog Fault Simulation
2. Modeling Methodology overview
3. Test Circuits and results
4. Future Work and Conclusion

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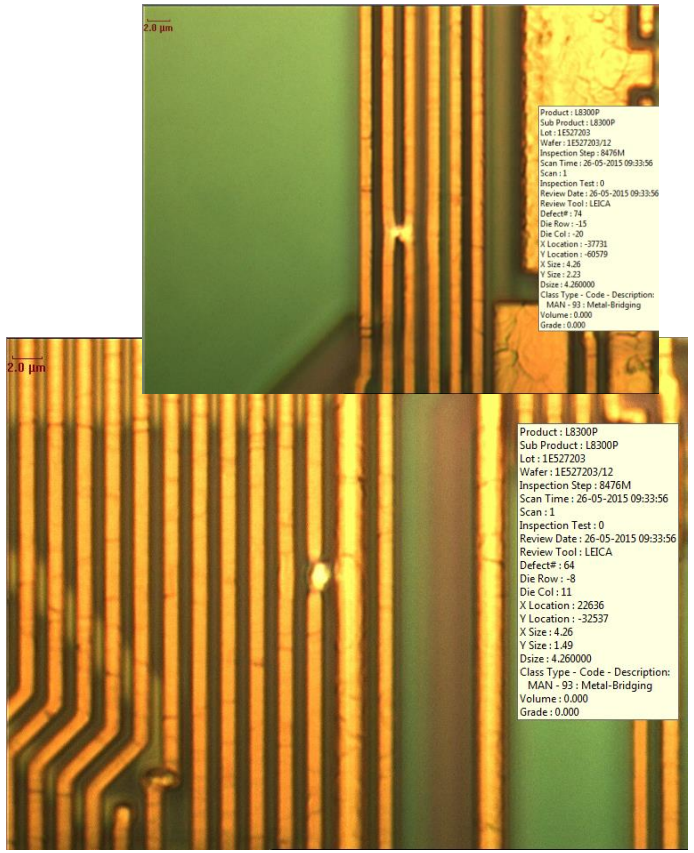
Motivation

- Several field returns (metal shorts, opens), which were not detected by the ATE test program
- Optimize test time and cost for circuits by evaluating the test program in regard of over-testing and under-testing
- Formally report and proof test coverage to customers
- Compliance to IEEE standard (working group IEEE p2427)

Avoid delivering such a circuit

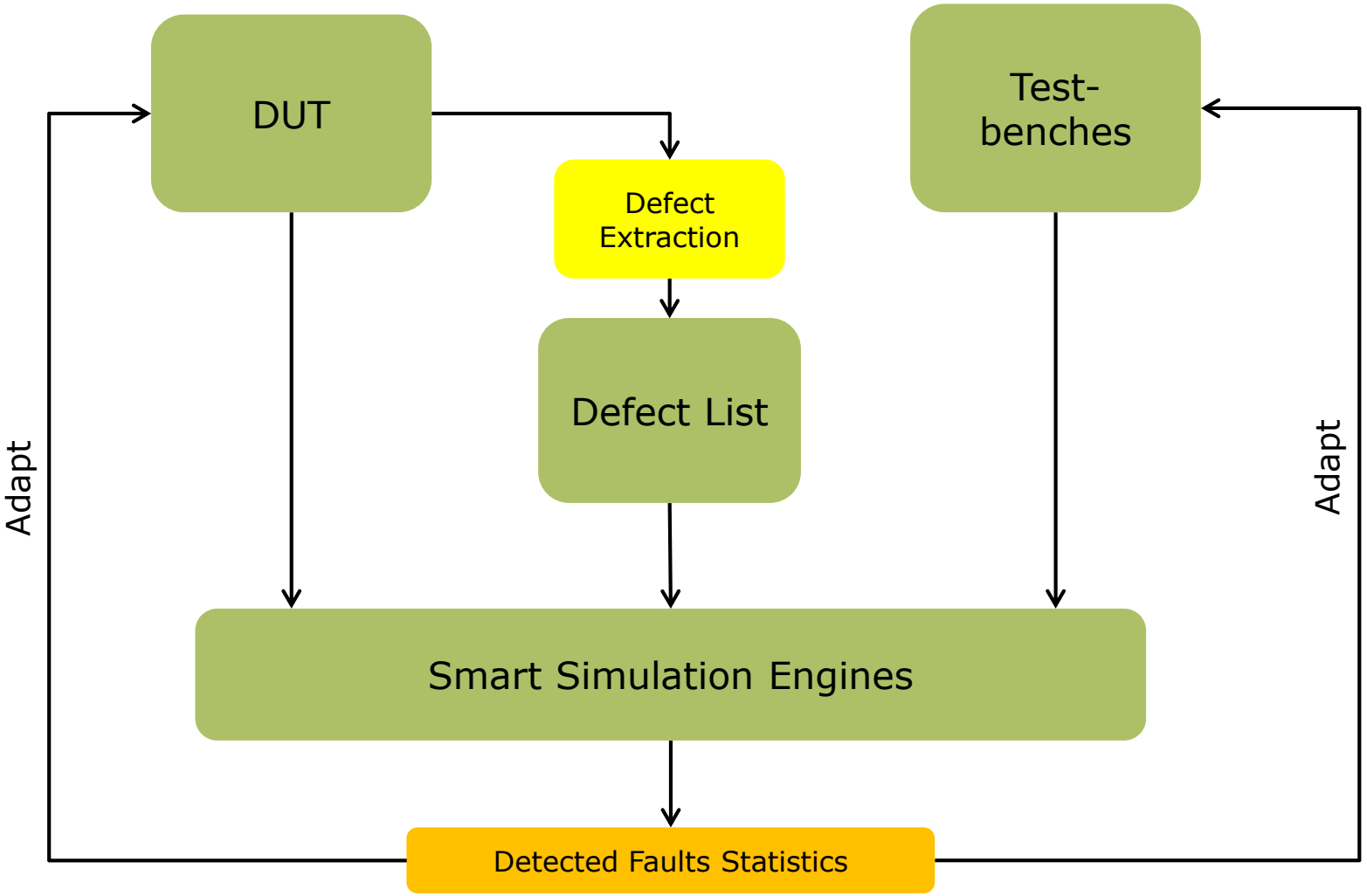


Example: Field return

Side Benefits

- In the functional safety domain, inject the defects in the fault catalog and check whether the safety mechanisms are excited
- Qualify the Design For Test(DFT) circuitry with defect coverage metric
- Testbenches qualification in mixed-signal verification

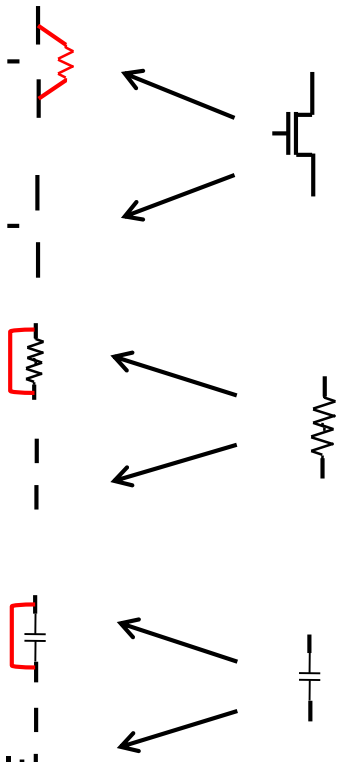
First Preliminary Flow Proposal



Fault models

Schematic

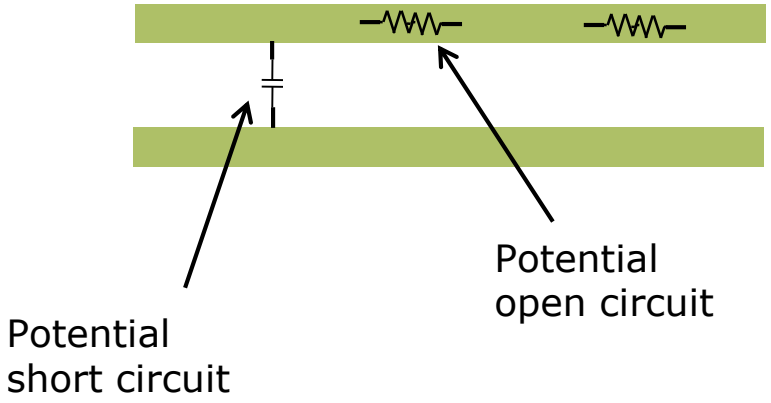
- Transistor
  - Stuck-at-on
  - Stuck-at-off
- Resistance
  - Short
  - Open
- Cap
  - Short
  - Open



- User Defined Faults
- Parametric defects

Layout

- Parasitic based fault extraction



Why is there no analog test coverage?

- A high side switch contains around 100k Transistors was examined in Infineon
- According to IEEE standard draft, open and short circuits are mandatory to simulate
- After excluding some complex blocks, all the digital part, and some metal layers and vias, total number of possible defects was over 50k.
- One simulation takes ~8 hours

„50,000 defects → **years** of simulations and high licenses cost”

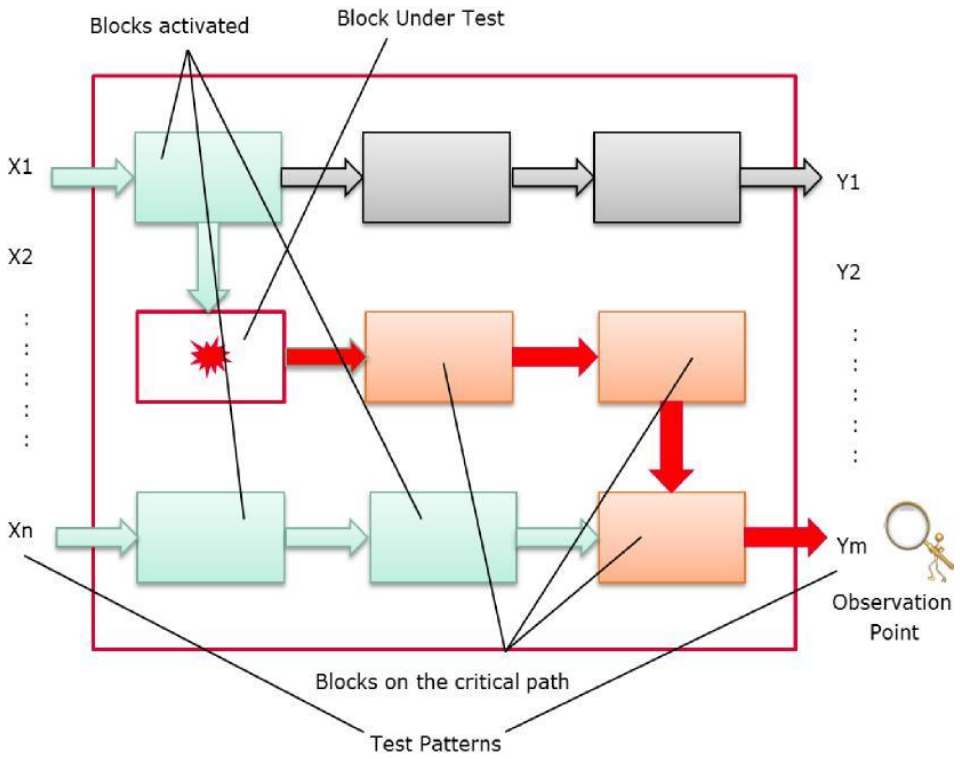
Simulation speed up

- Parallel Defect Simulation
- Fault Collapsing
- Random Sampling of the defects to estimate the coverage with certain confidence.
- Fault Sensitivity Analysis (FSA)
- Define levels of detectability
  - Undetected, detected, and undetectable defects
  - Find worst corner for Process Voltage Temperature variation
- Start with the defects that have more likelihood and stop after a sufficient coverage is reached
- Simulating defects in abstract-level surrounding[Model the surrounding blocks where a defect is injected]

Using Models in AFS context

Definitions:

- Block under Test
  - Source block into which faults are injected
- Defect effect propagation path
  - From the source block to the observation point
- Blocks on the propagation path
  - Abstract models capable of propagating fault effect



Can the abstract models propagate the fault effect?

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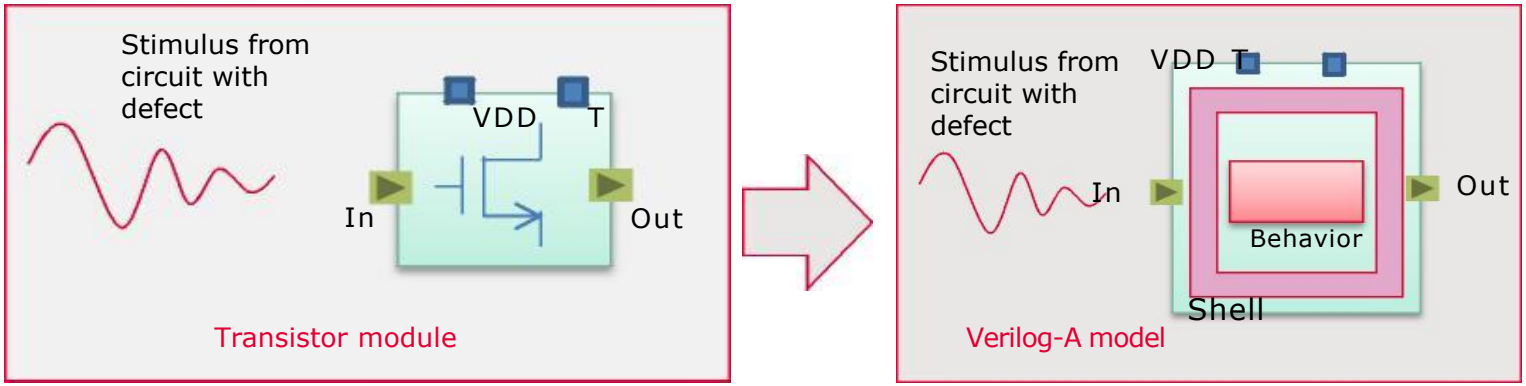
Overview of the Methodology

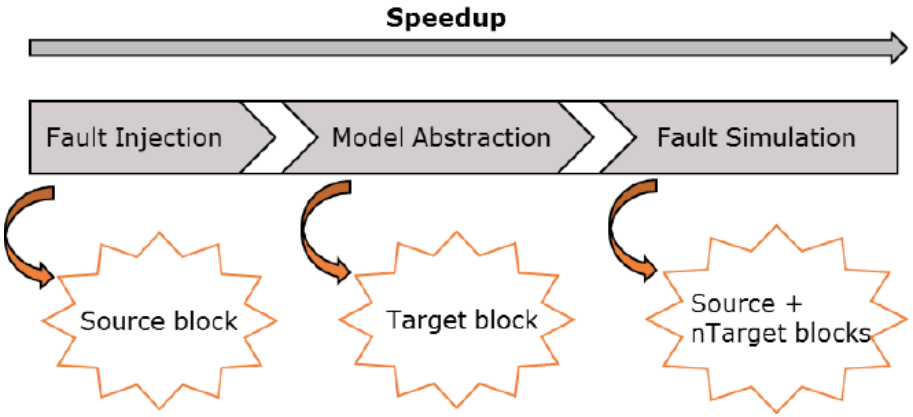
› Augment a shell to the model that covers the fault effects



$$Accuracy(in\ \%) = \frac{Measure_{(Transistor\ model)} - Measure_{(Abstract\ model)}}{Measure_{(Transistor\ model)}} * 100$$

$$Speedup\ Factor = \frac{Simulation\ Time\ _{(Transistor\ model)}}{Simulation\ Time\ _{(Abstract\ mode)}} * 100$$

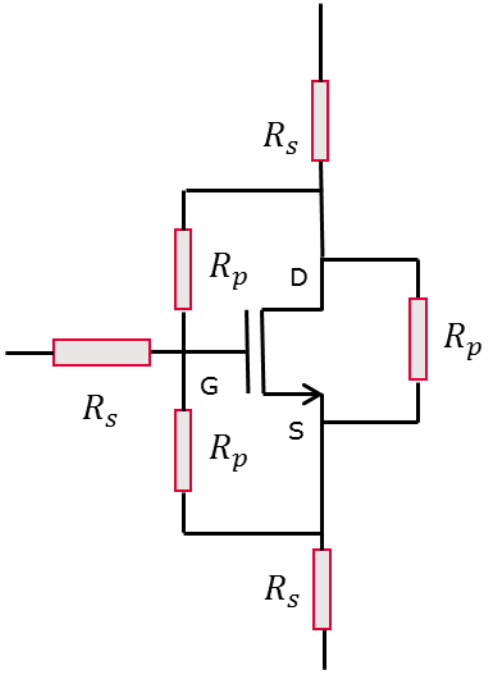
Overview of the Methodology



- Fault injection on the source block
  - To identify the fault effects to propagate
- Target block Model abstraction
  - Model augmented with fault effects
- Fault simulation
  - With source block and abstract models to speed up the simulation

Fault Injection

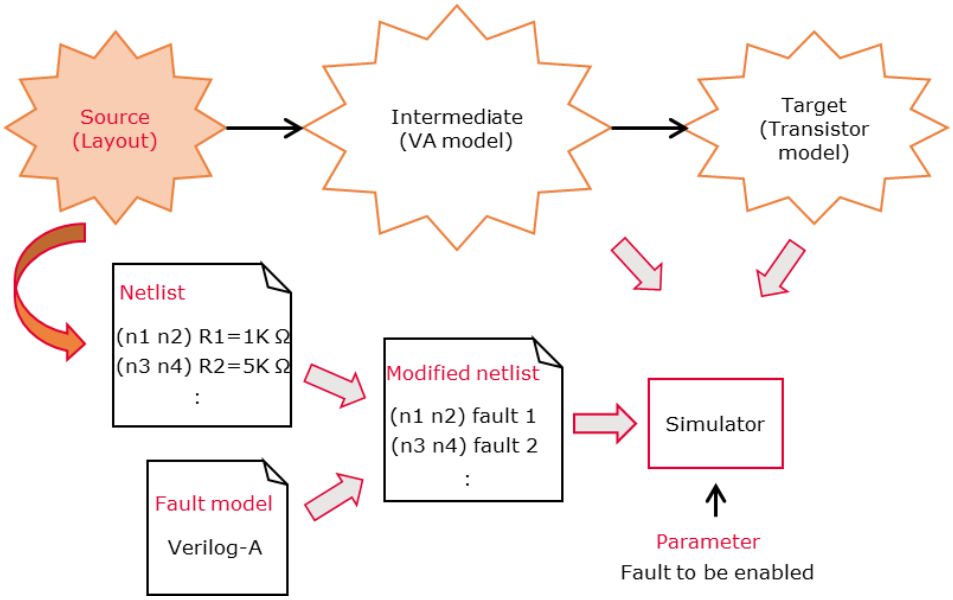
› Fault model



› Fault extraction from the transistor level

  – Large number of faults

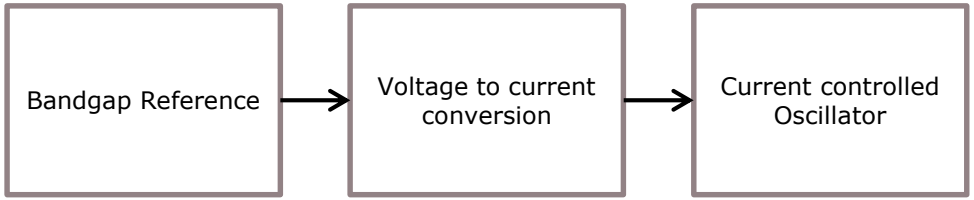
› Fault injection flow

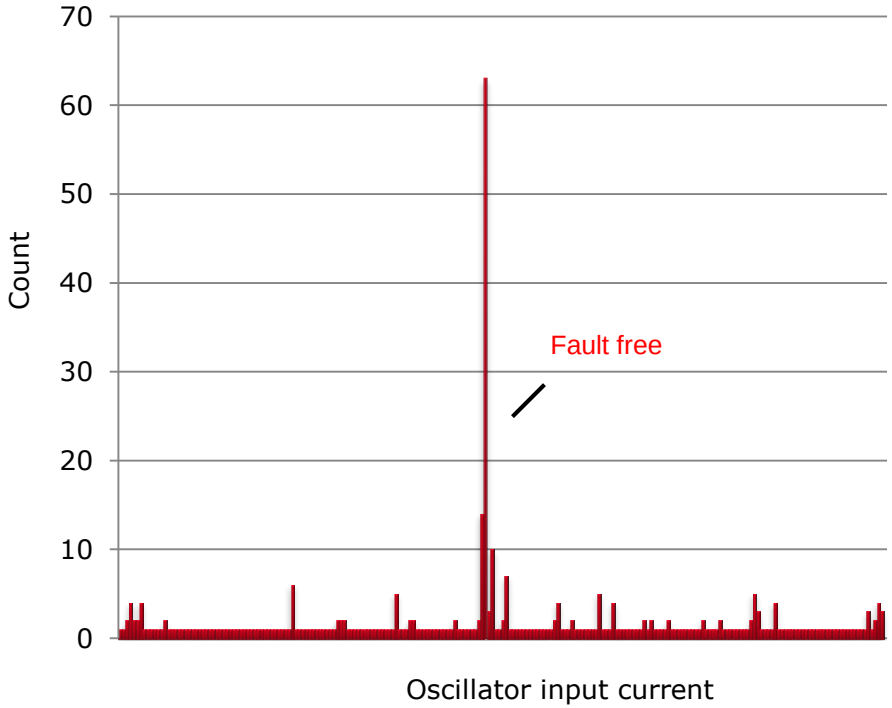


› Possible faults extracted from the layout

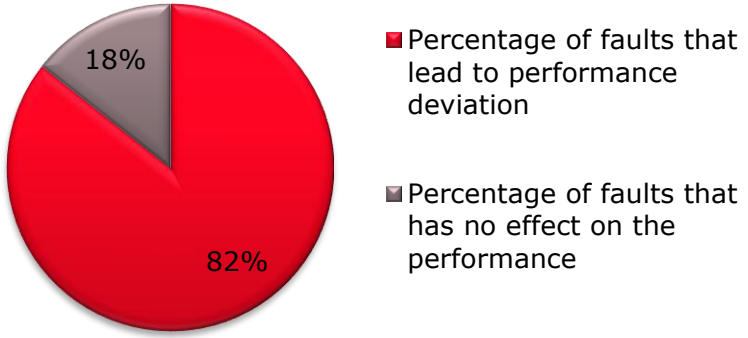
› Batch mode simulation in Regression environment

Fault list generation and reduction



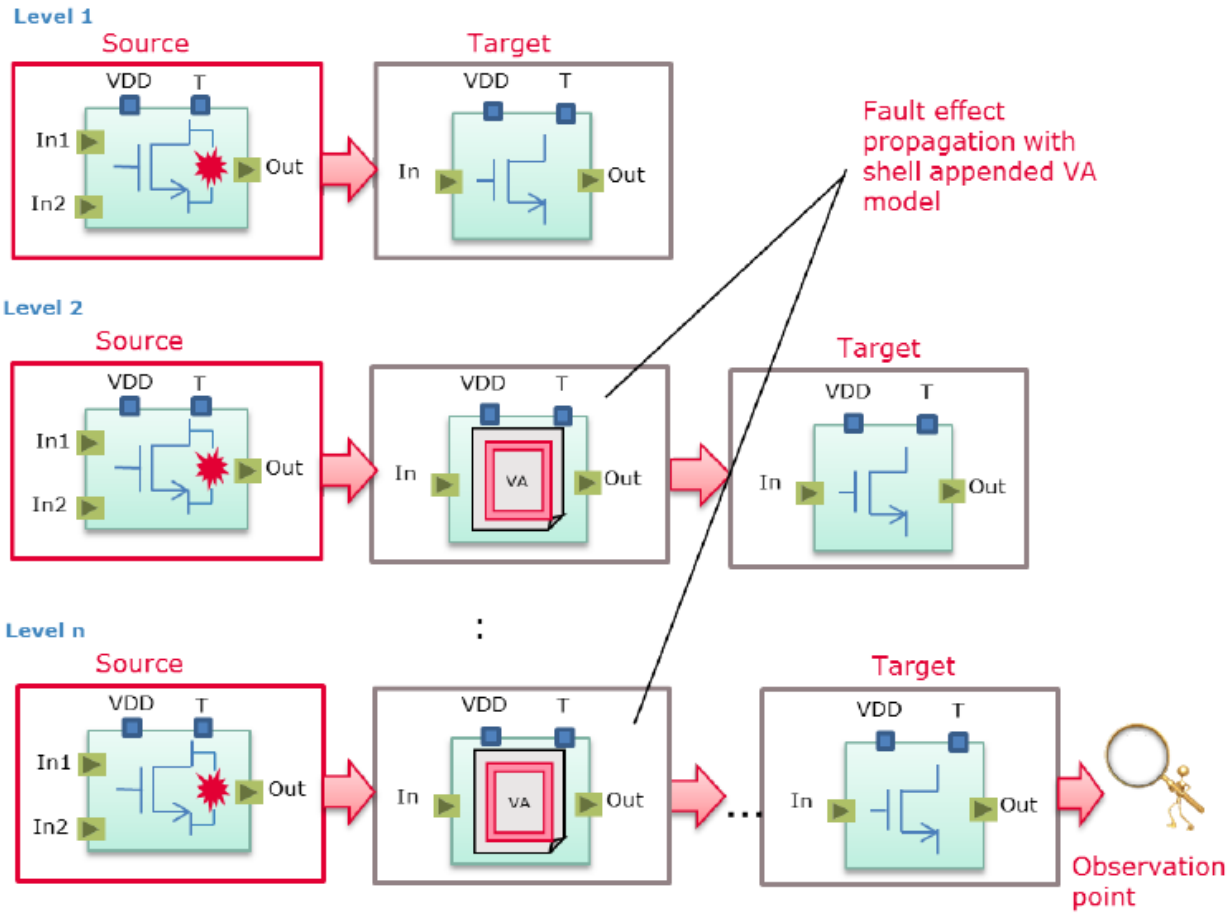


Parameter	Value
Number of Parallel simulation	40
Number of faults simulated	375
Fault type	Short
Fault resistance	10 Ω



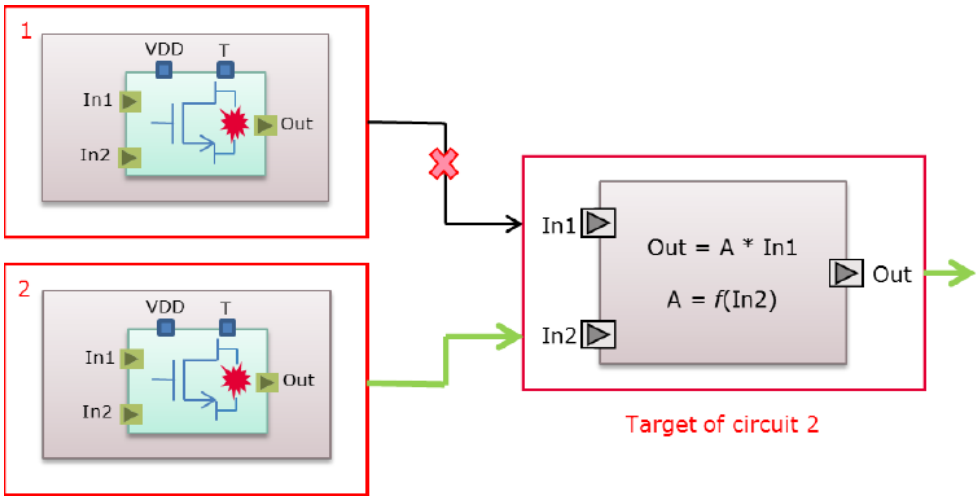
Model abstraction in steps

- One target block at a time to model

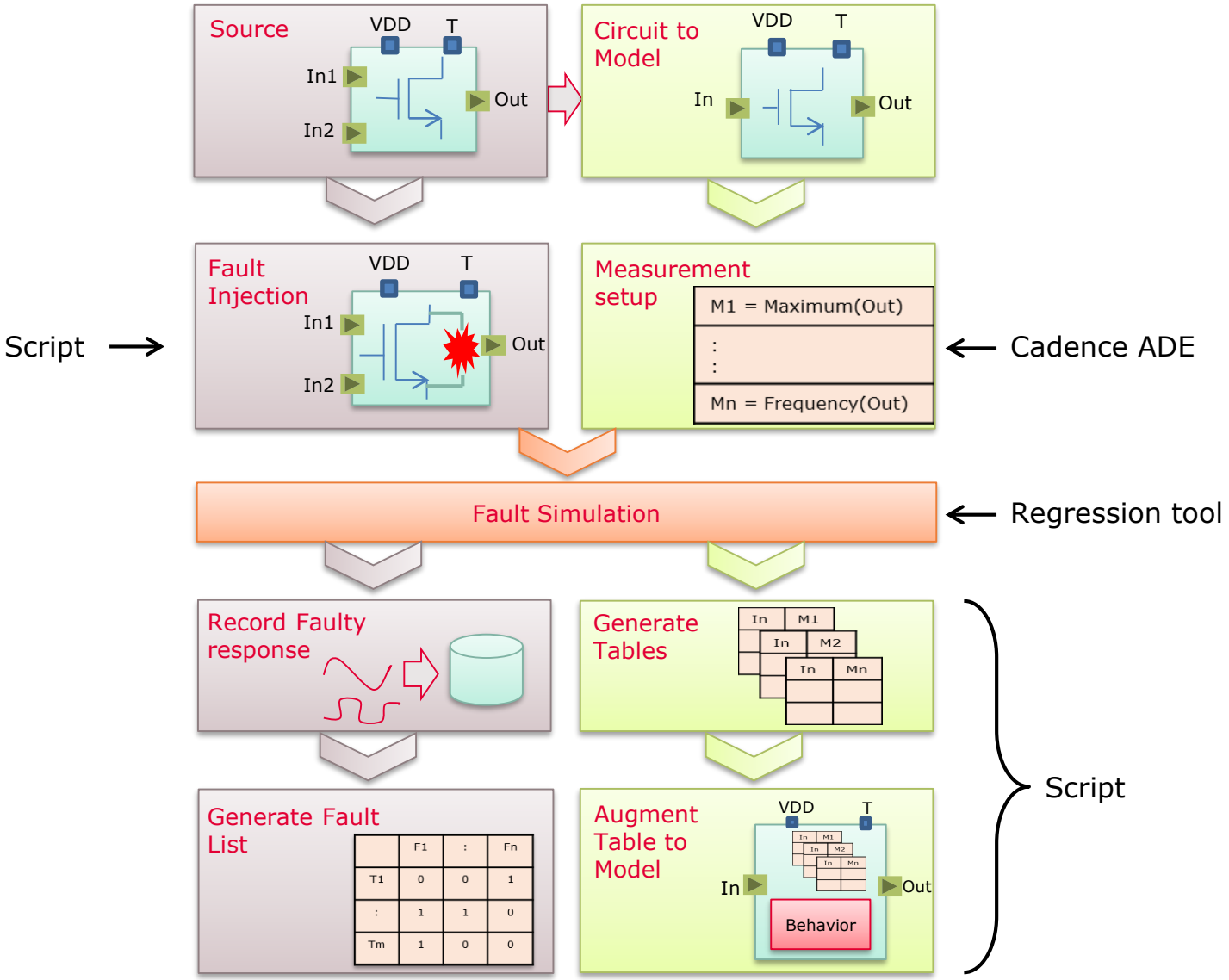


Exclude some blocks

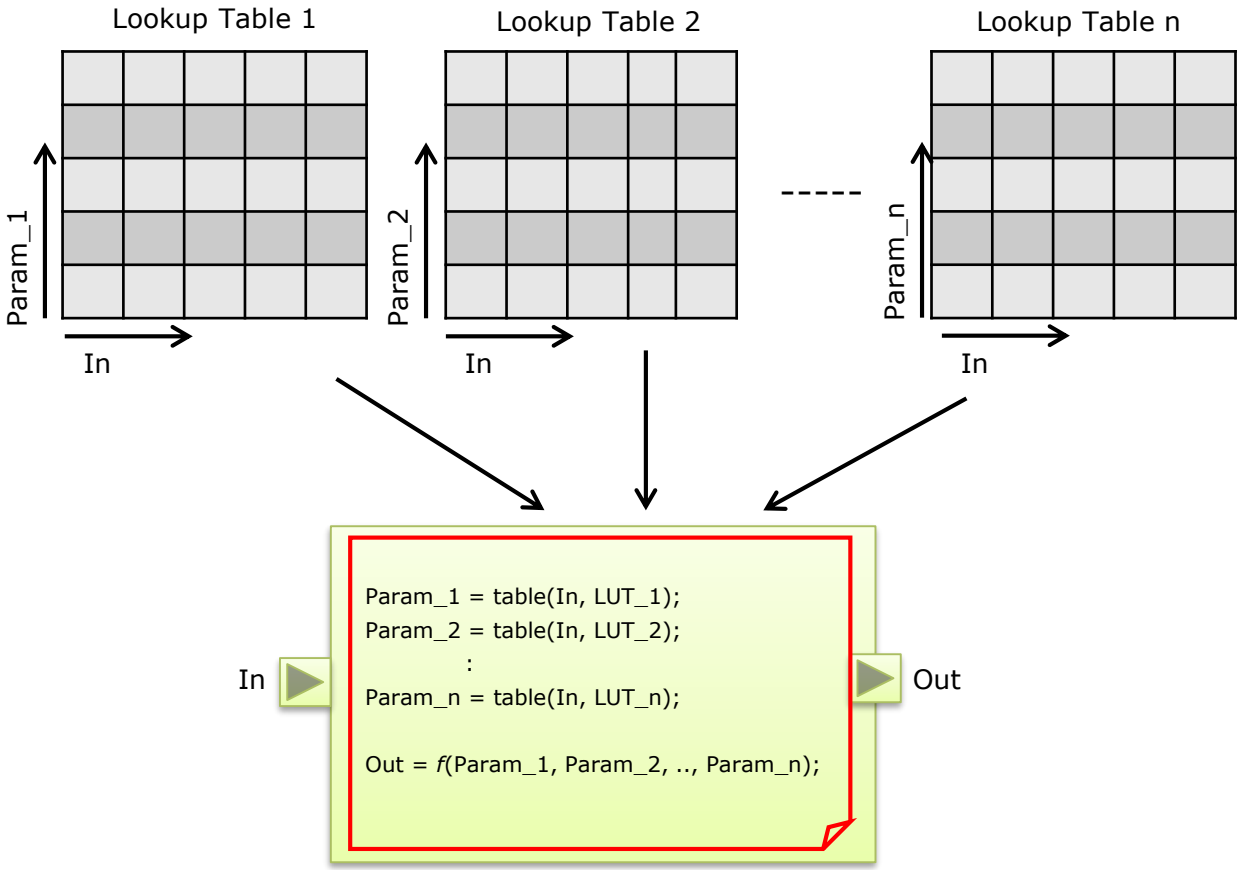
- Do all the target blocks require shell to include fault effects ?
  - Target circuit selection
- Some circuits propagate faults without any shell
  - Analog switch



Model abstraction



Mapping with Look-Up Tables



Measurements are done on the continuous signals

- Need for interpolation (in the case of slight variation in the input value)

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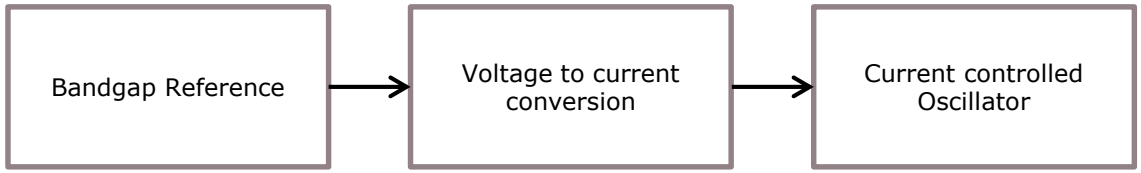
Experiment Result

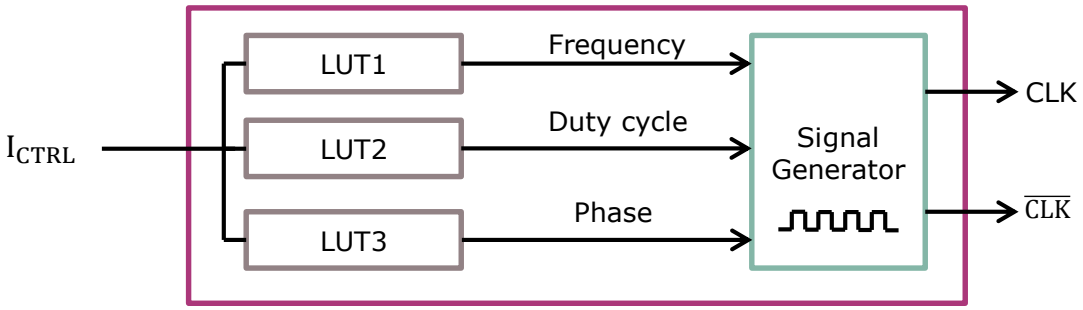
› Experiment setup



› Parameters chosen for measurements

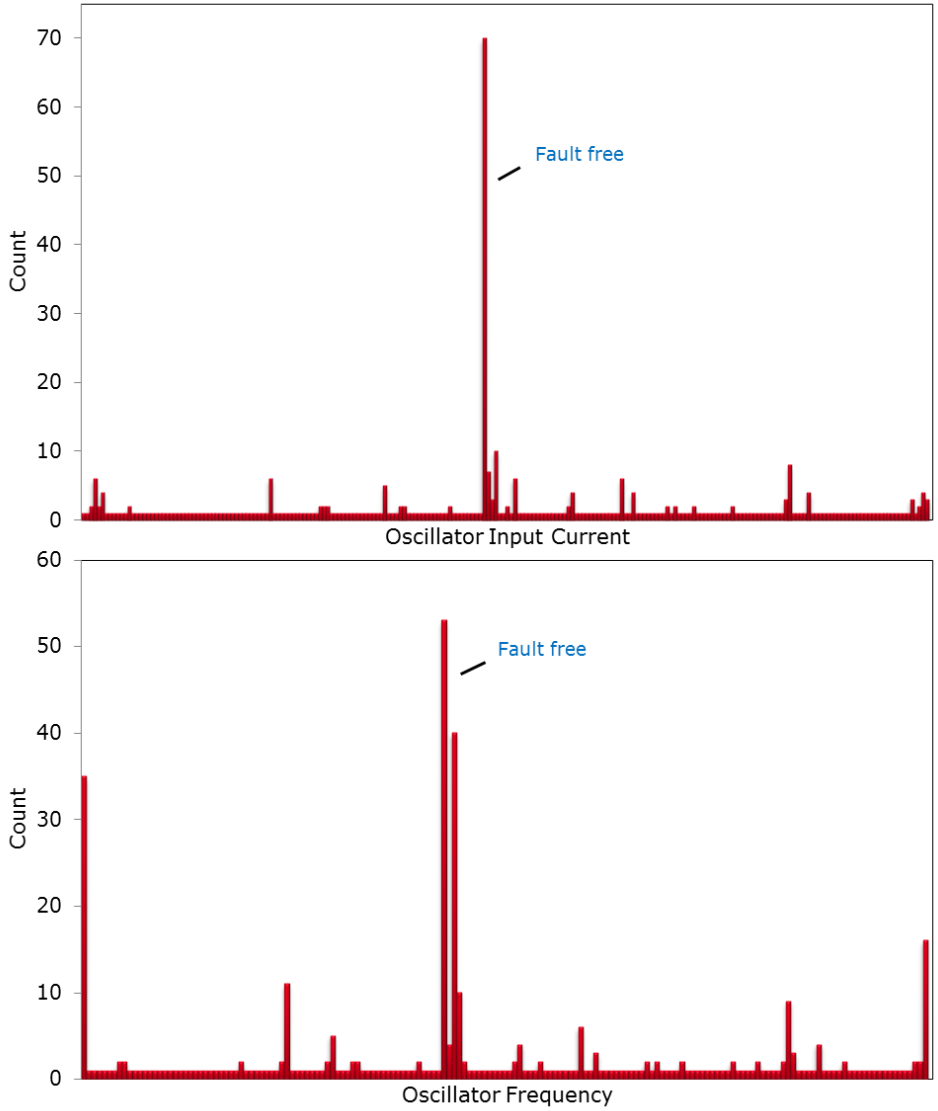
Input Parameters	Output Parameters
Supply Voltage	Frequency
Temperature	Duty cycle
Input reference current	Phase
Load resistance	Rise time
	Fall time
	Average output voltage

› Oscillator model with Look-Up Tables

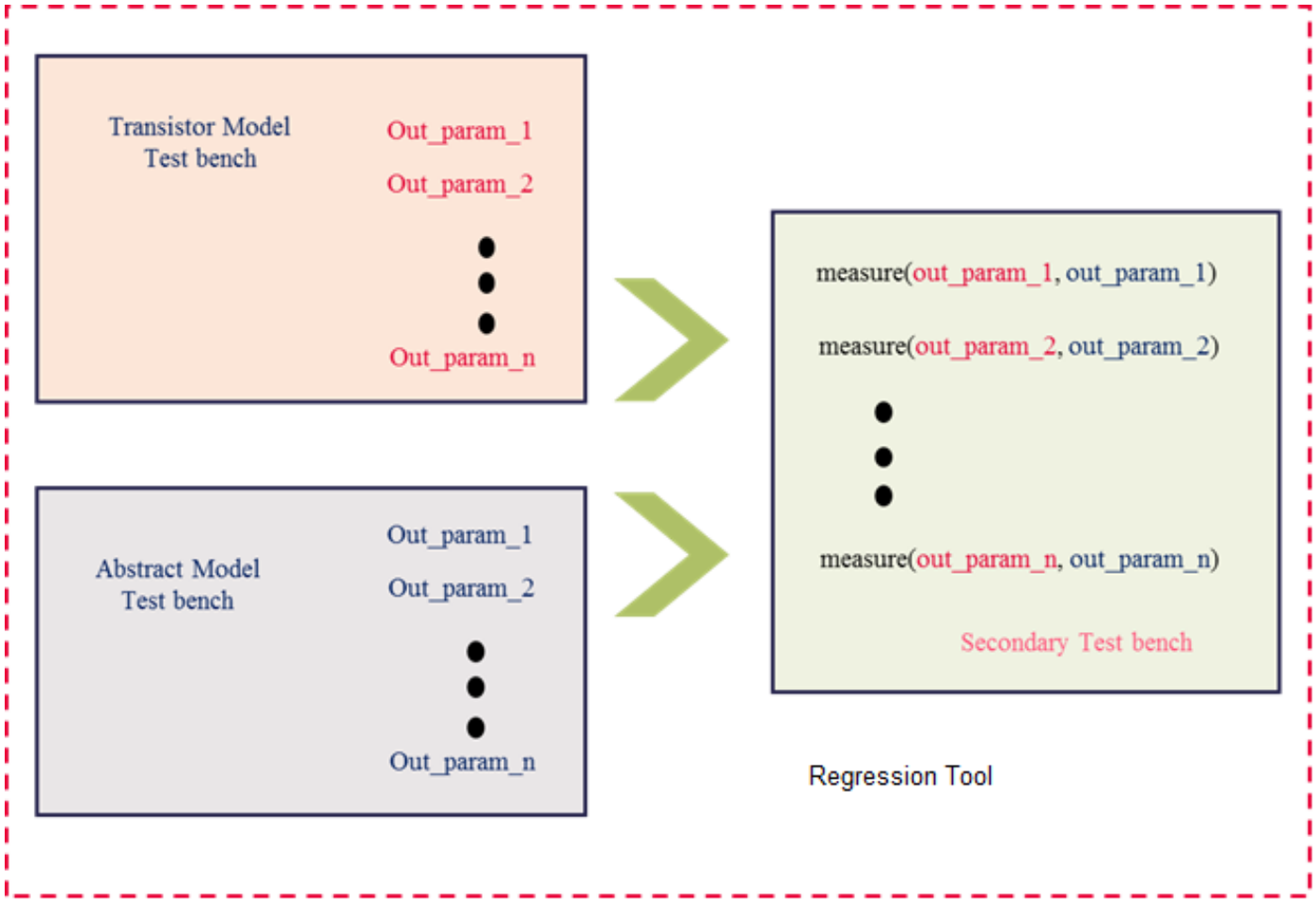


Model parameters distribution vs defects

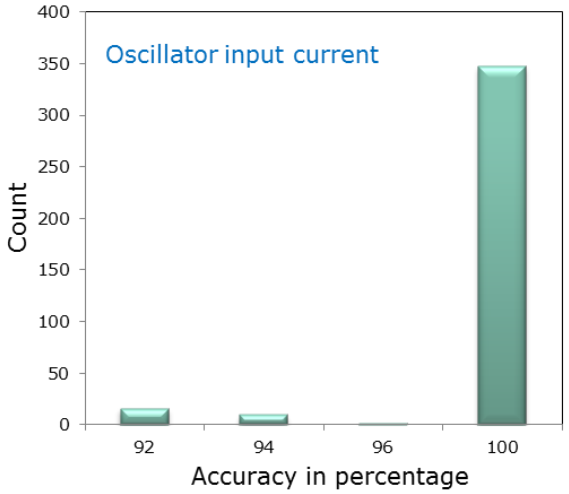
- The distribution of Oscillator input current and its frequency for faults injected in Bandgap Reference Circuit

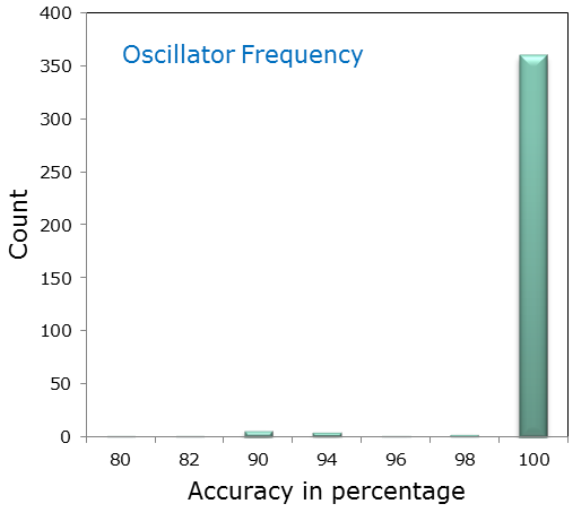


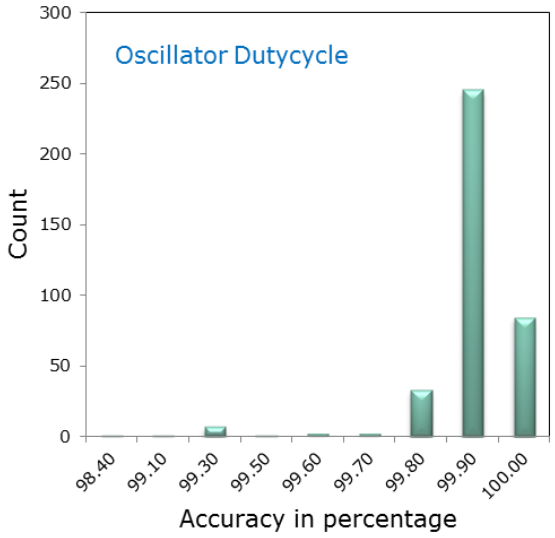
Equivalence Checking

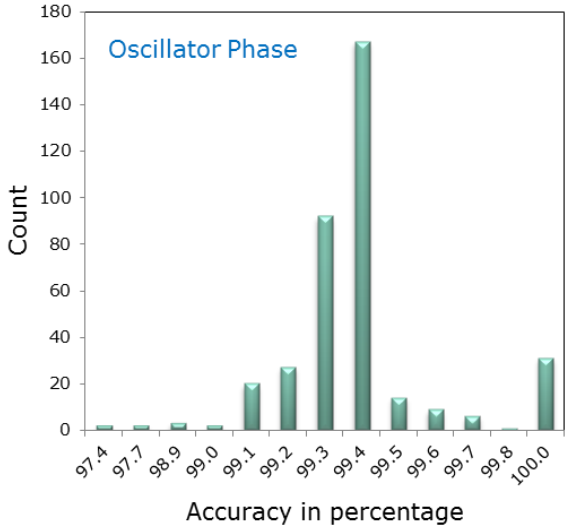


Experiment Result



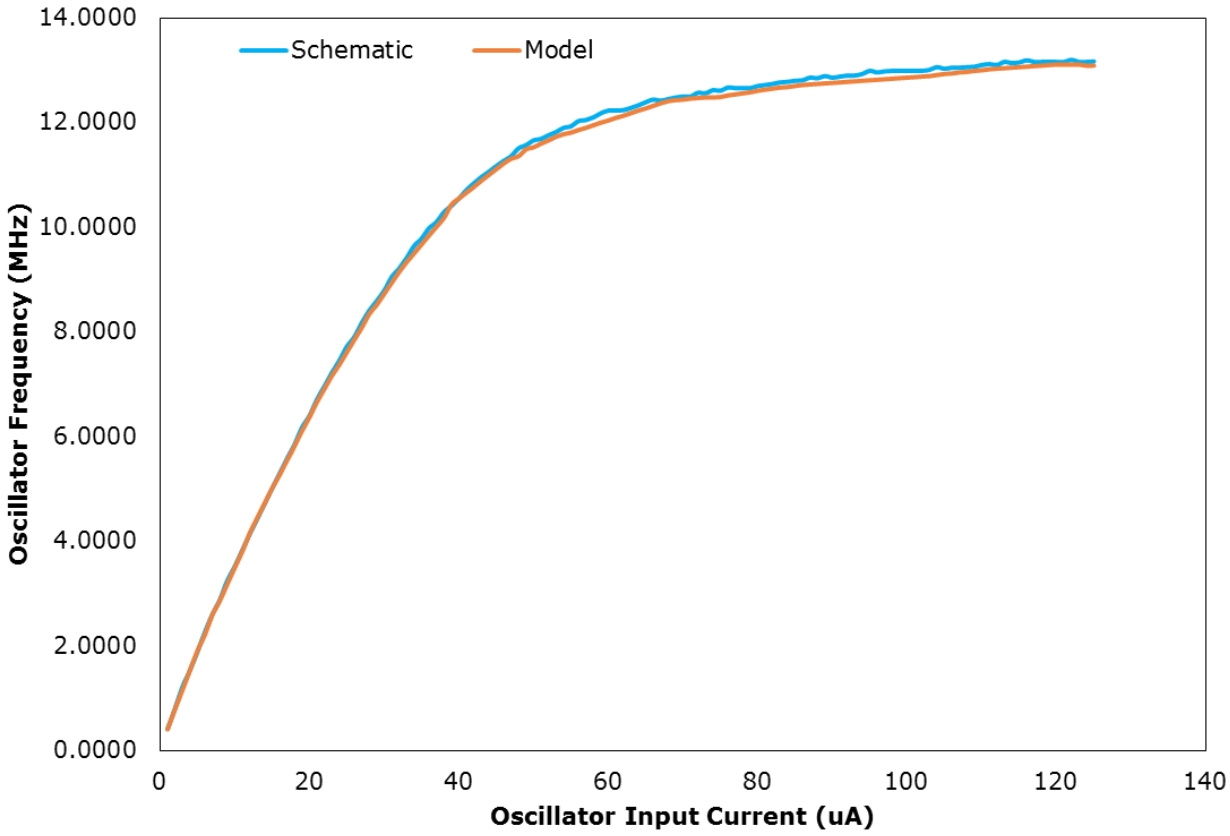






Experiment Result

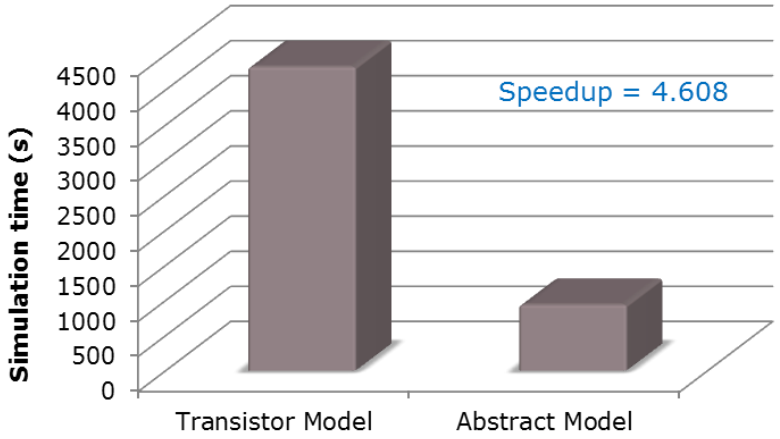
Interpolation accuracy



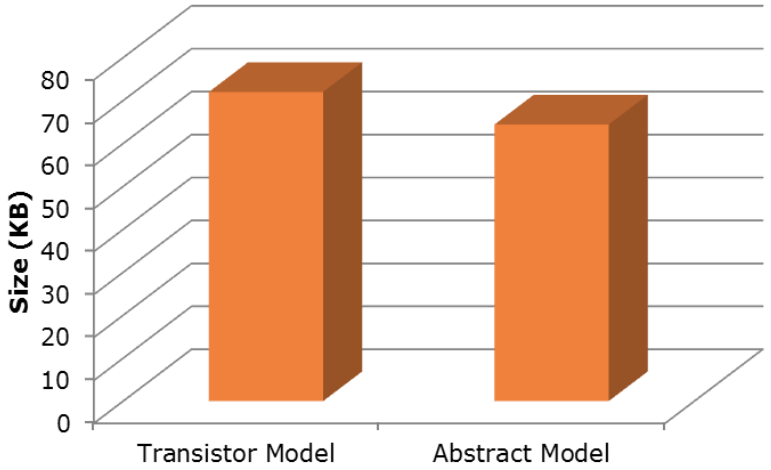
Interpolation accuracy for the input reference current sweep with step size 1uA

Experiment Result

Parameter	Value
Transient simulation time	3 us
Time step	100 ps
Number of Parallel simulation	40
Number of faults simulated	375
Fault type	Short
Fault resistance	10 Ω



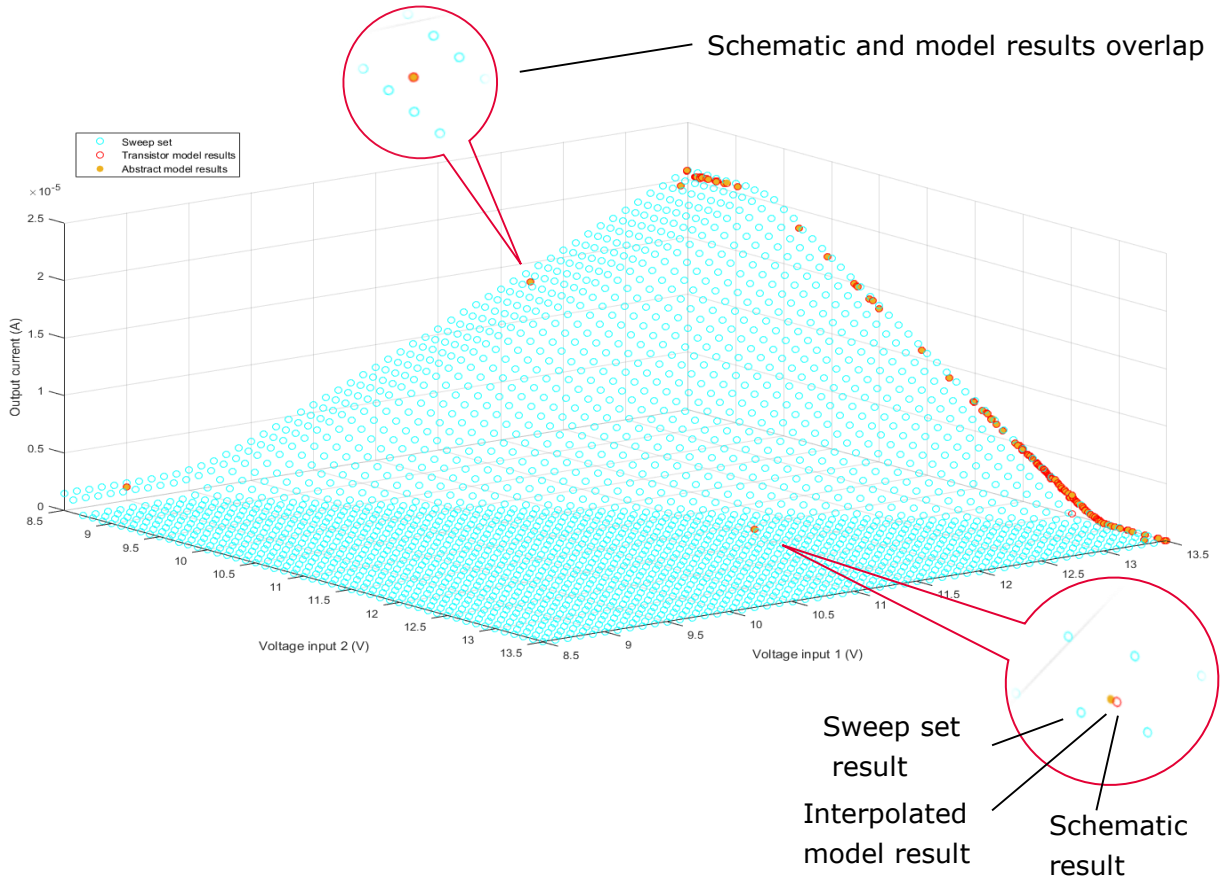
Simulation time : Transistor model vs Abstract model



Storage : Oscillator's Schematic vs its Model with LUTs

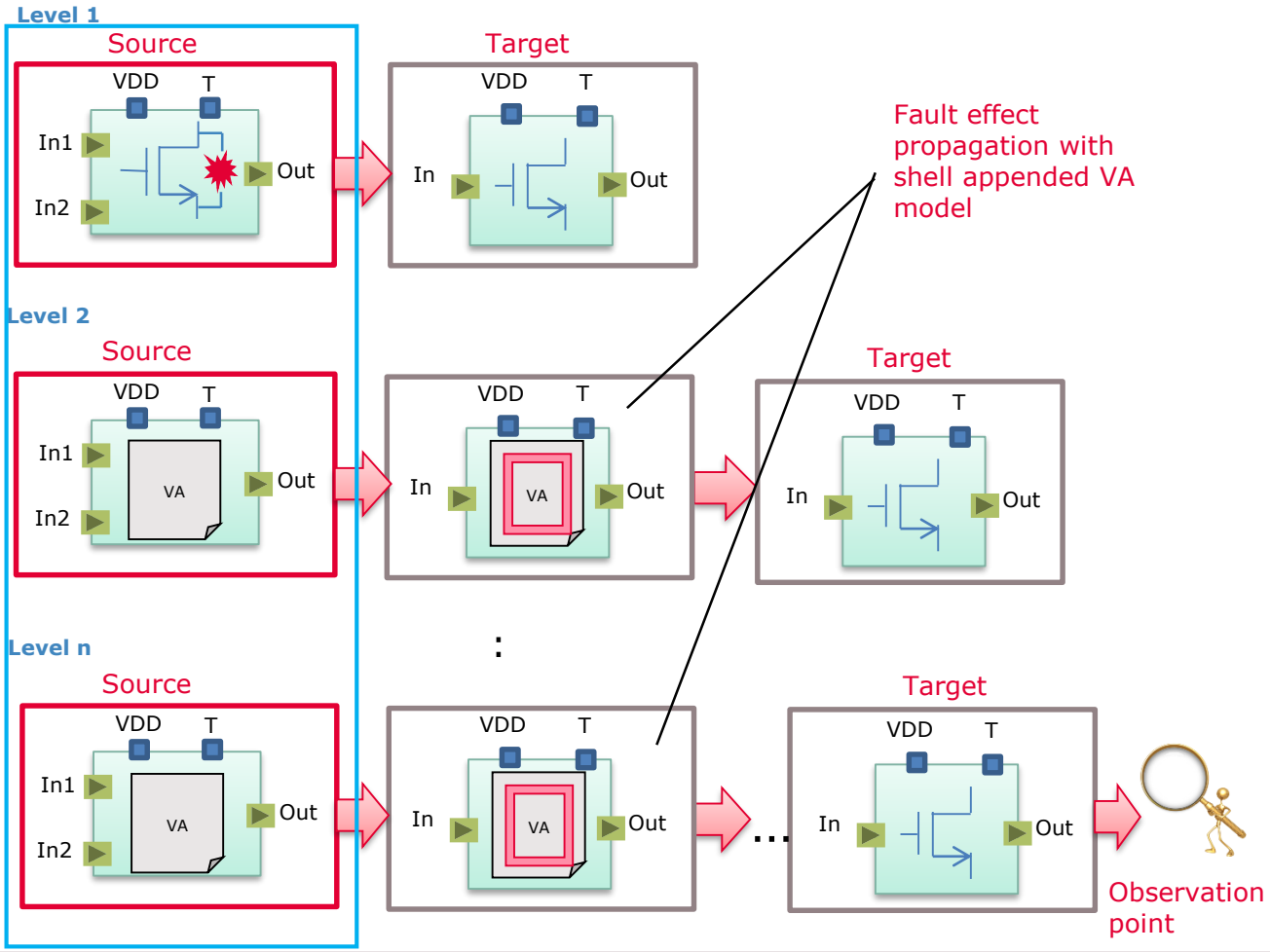
3D Mapping of the parameters depending on multiple inputs

The voltage-to-current takes two inputs from Bandgap Reference circuit and outputs a current that controls the Oscillator

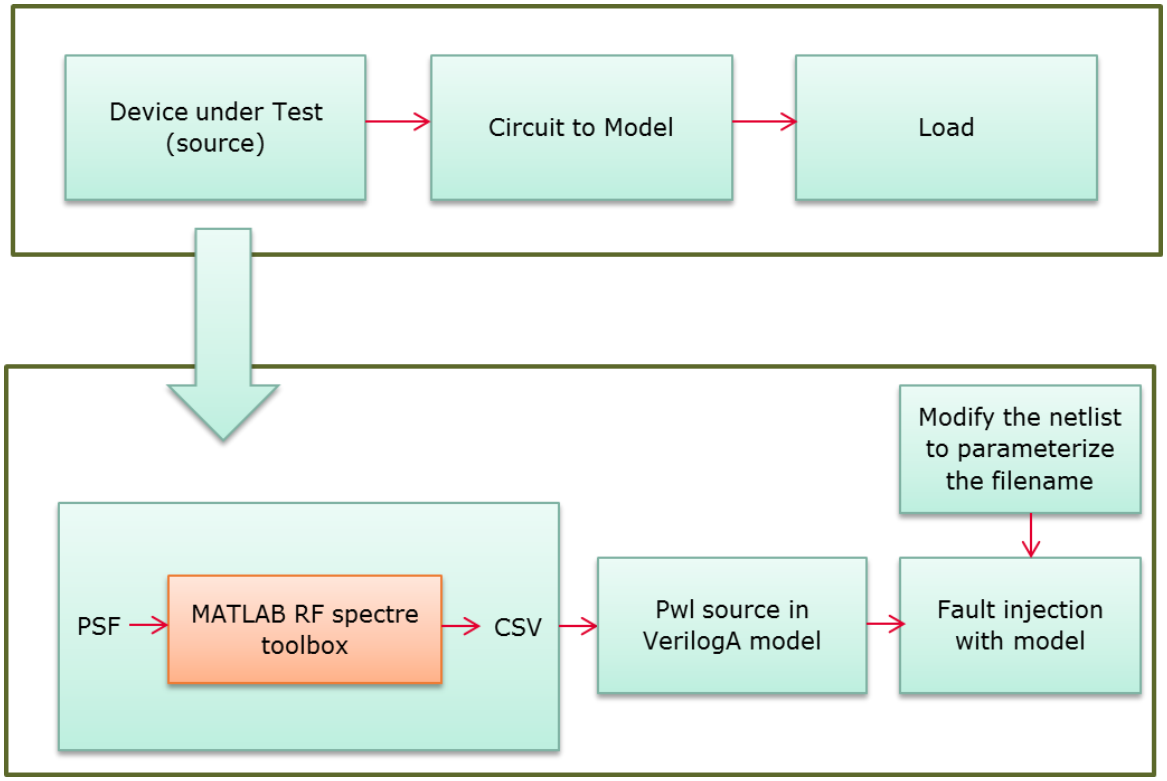


Using the Abstract Models for fault injection

- To speed up the process of generating abstract models (target blocks)



Modified Flow and its Result



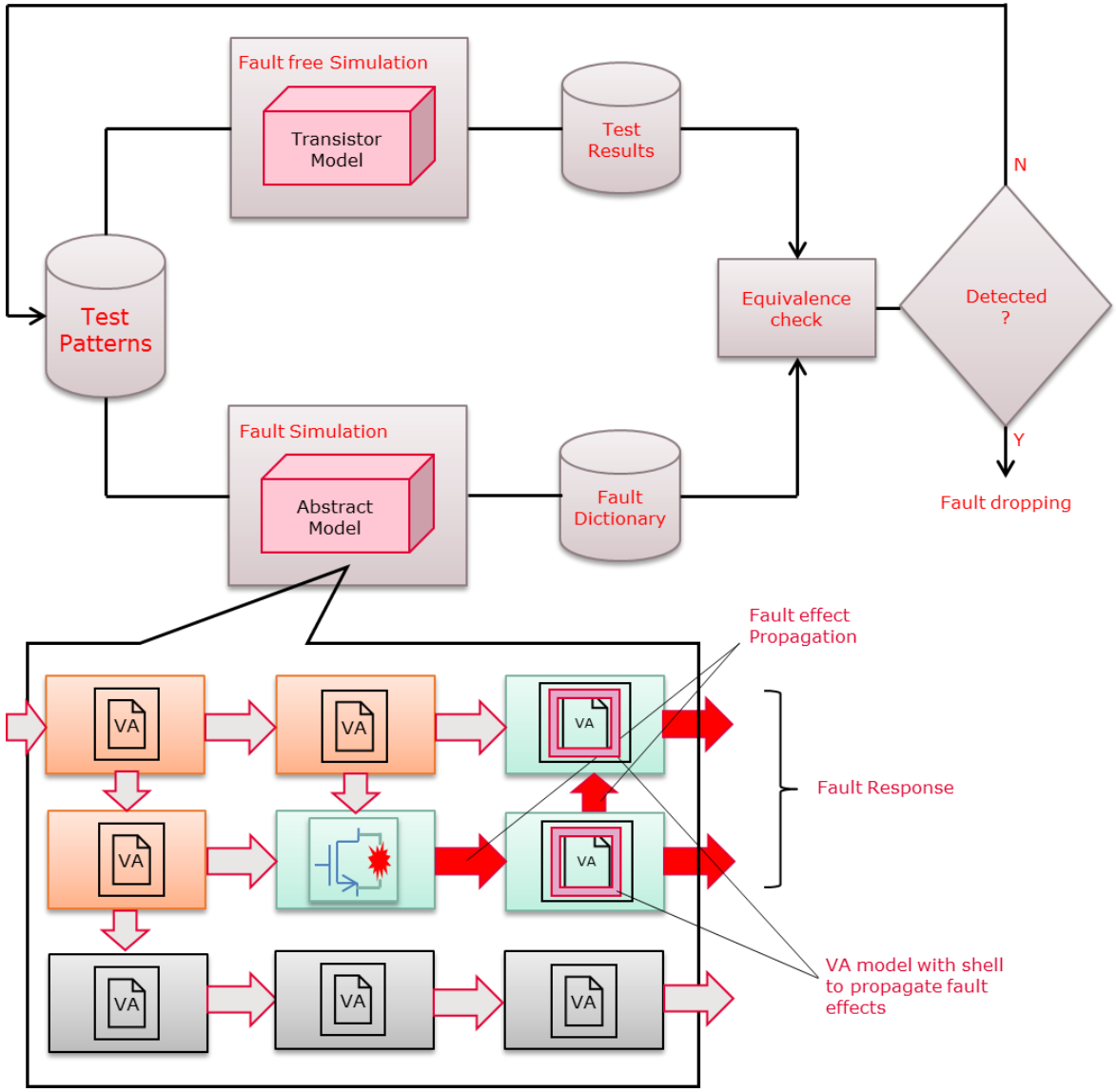
Flow to generate Fault model of a circuit

Experimental results

Parameters	Value
Number of Faults simulated	100
Simulation time	50 us
Time step	100 ps
Number of parallel runs	40
Speed up	10x

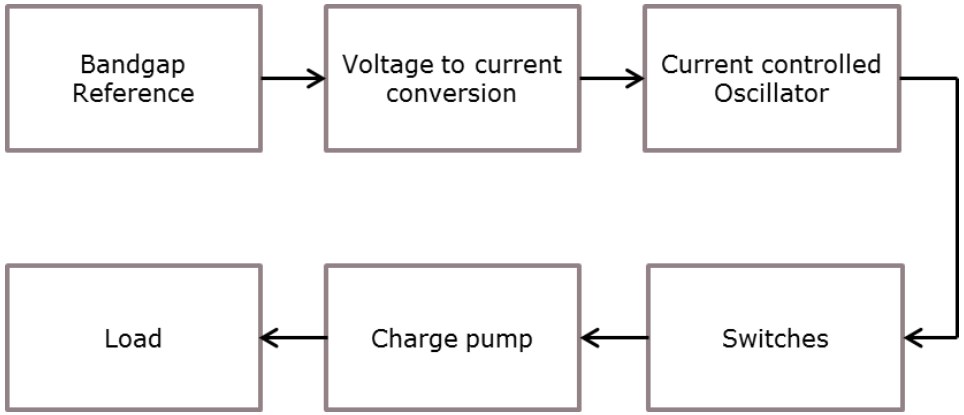
› Storage of CSV files

Fault Simulation - Flow



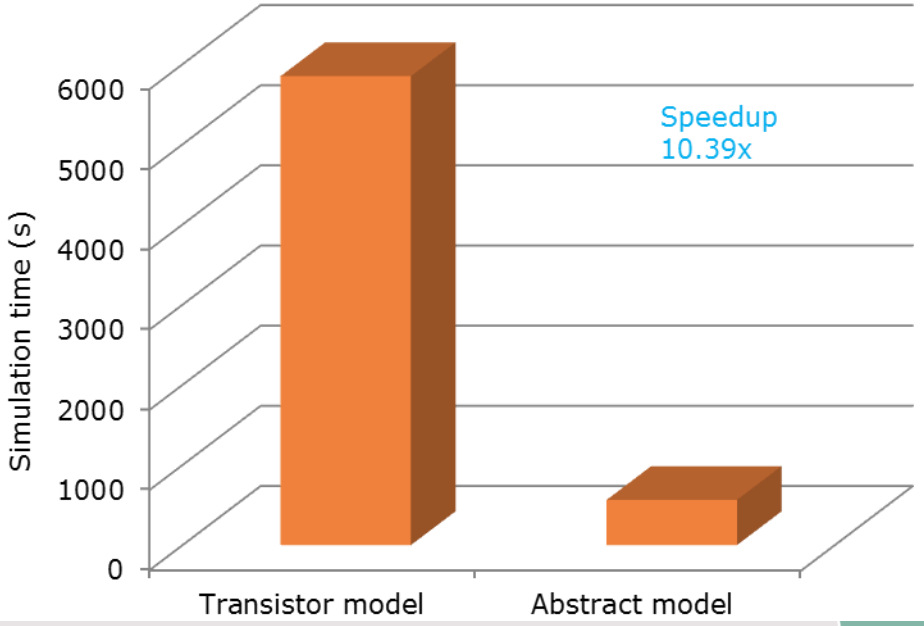
Fault Simulation – Full chain

Blocks on the target path



Experiment Setup

Parameter	Value
Transient simulation time	5 us
Time step	100 ps
Number of Parallel simulation	40
Number of faults simulated	375
Fault type	Short
Fault resistance	10 Ω

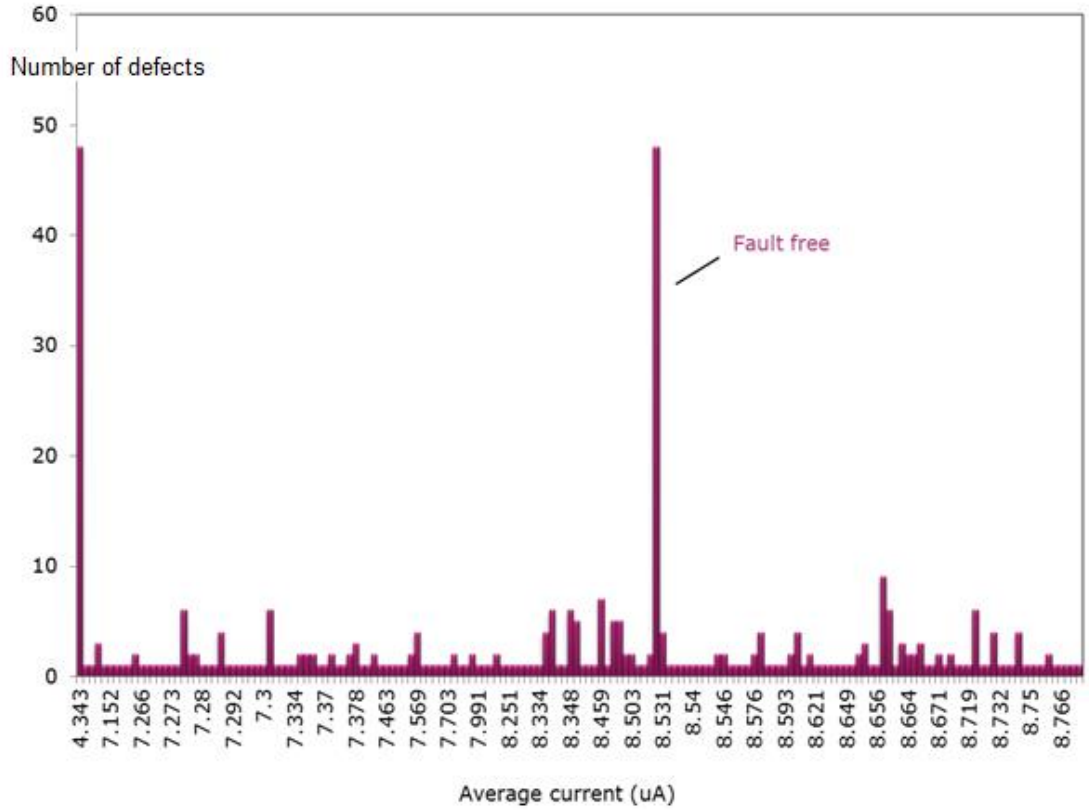


Fault Simulation – Experiment Result

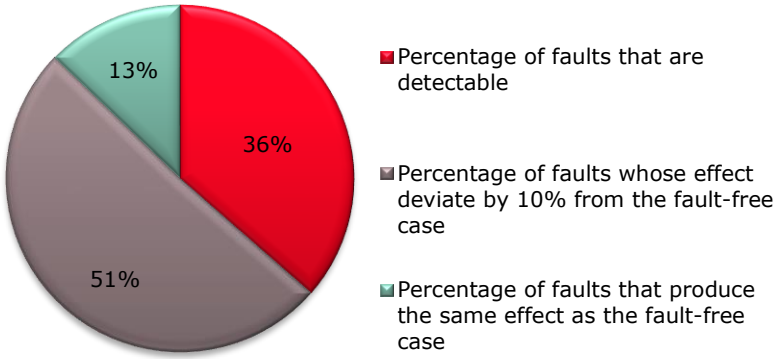
Parameter	Value
Transient simulation time	20 us
Time step	100 ps
Number of Parallel simulation	40
Number of faults simulated	375
Fault type	Short
Fault resistance	10 Ω

Full simulation time – 35 mins (app)

Distribution of the average current measured at the load



Fault detection results



36% - faults dropped

64% - Different test pattern must be chosen to detect these faults

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Conclusion and Future Work

- AFS at the system level
- Abstract models to speed up AFS
- Fault effect propagation with shell appended behavior models
  - Performance metrics mapped to faulty inputs using LUT
  - Multi-dimensional mapping
  - Applicable to Closed-loop systems

Performance results

- A simple, multi-dimensional, LUT mapping with interpolation
- Speedup of about 10 times
- Accuracy close to 100%
- Storage size in few KBs

Future Work

- Propagation path tracing using Sensitivity analysis
- Fault collapsing using clustering algorithms
- Automation of Model abstraction and Fault simulation at the System level

References

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[2] Mark Zwolinski, Andrew D. Brown, "Behavioural modelling of analogue faults in VHDL-AMS - a case study", Circuits and Systems, Proceedings of the 2004 International Symposium on 2004, ISCAS ’04, May 2004.

[3] Jyotsna Sequeira, Suriyaprakash Natarajan, Prashant Goteti and Nitin Chaudhary, "Fault Simulation for Analog Test Coverage", Test Conference (ITC), 2016 IEEE International, Nov 2016.

[4] Ramin M. Hasani, Dieter Haerle, Radu Grosu, "Efficient Modeling of Complex Analog Integrated Circuits Using Neural Networks", 2016 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), June 2016.

[5] Ender Yilmaz, Geoff Shofner, LeRoy Winemberg, Sule Ozev, "Fault analysis and simulation of large scale industrial mixed-signal circuits", Design, Automation & Test in Europe Conference & Exhibition (DATE), March 2013.

[6] Z.R. Yang, M. Zwolinski, "Fast, robust DC and transient fault simulation for nonlinear analogue circuits", Design, Automation & Test in Europe Conference & Exhibition (DATE), March 1999.

[7] Joonsung Park, Srinadh Madhavapeddi, Alessandro Paglieri, Chris Barr and Jacob A. Abraham, "Defect-Based Analog Fault Coverage Analysis using Mixed-Mode Fault Simulation", IMS3TW ’09. IEEE 15th International Mixed-Signals, Sensors, and Systems Test Workshop, June 2009.

Part of your life. Part of tomorrow.

Infineon

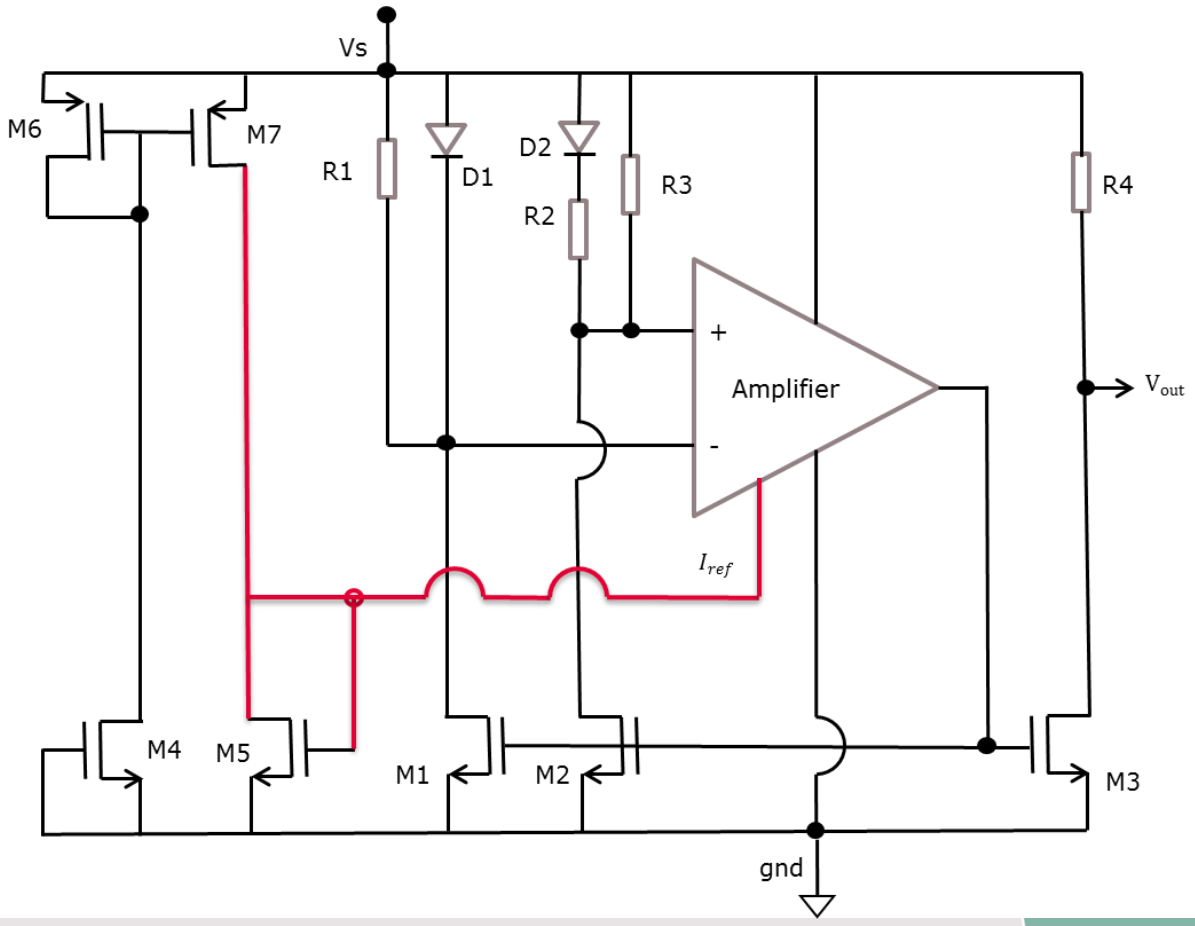
Closed loop system

Modeling the transient response as a time series

- Inefficient

Performance modeling

I_{ref} affects the performance of the Op-Amp



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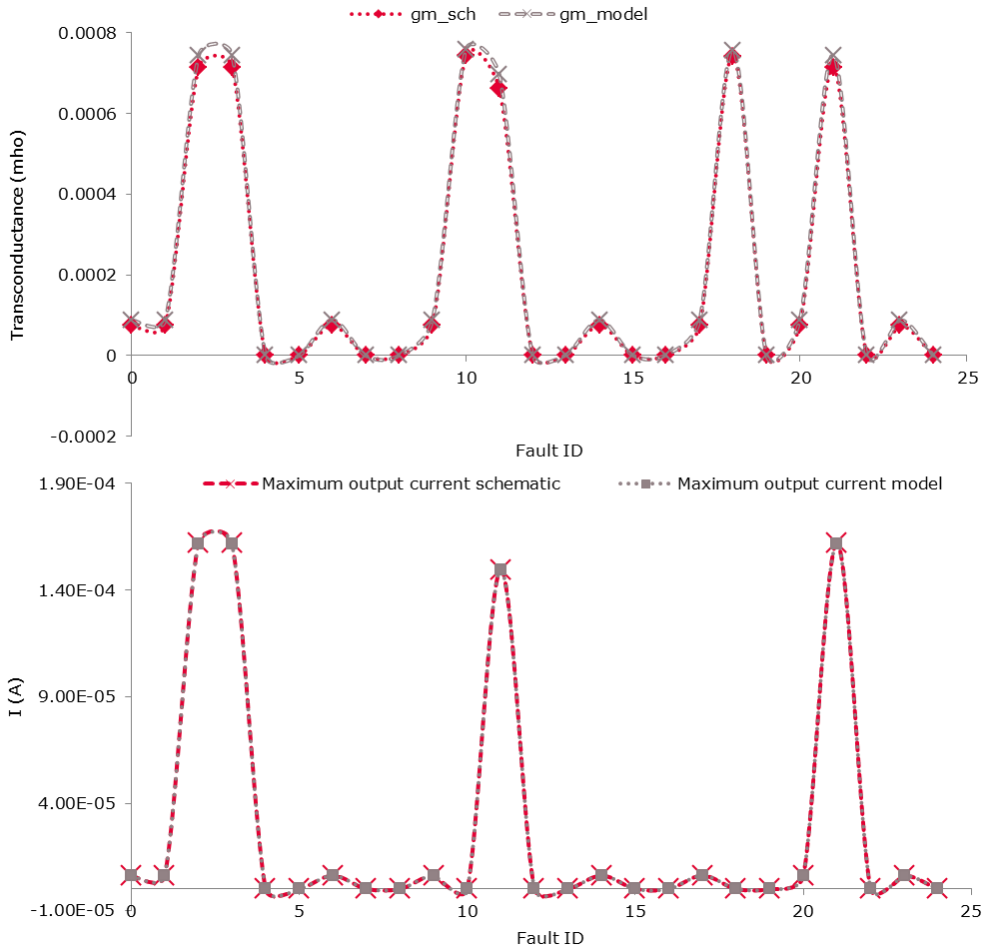
Closed loop system - Experiment Result

Equivalence checking



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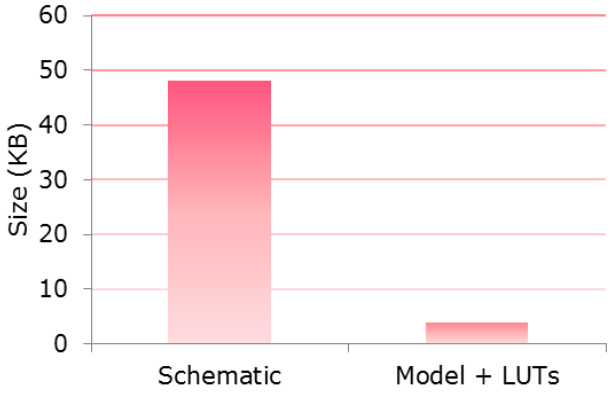
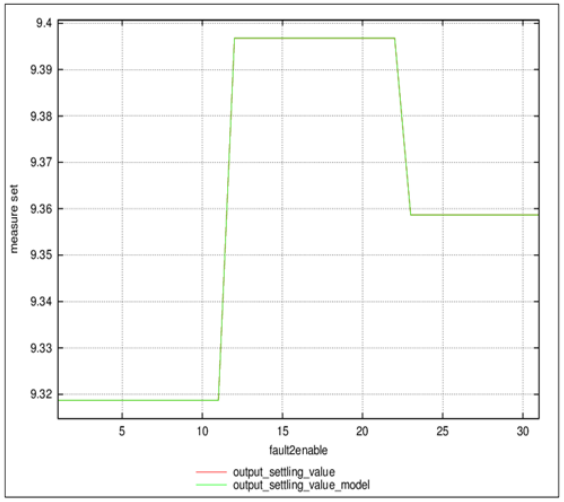
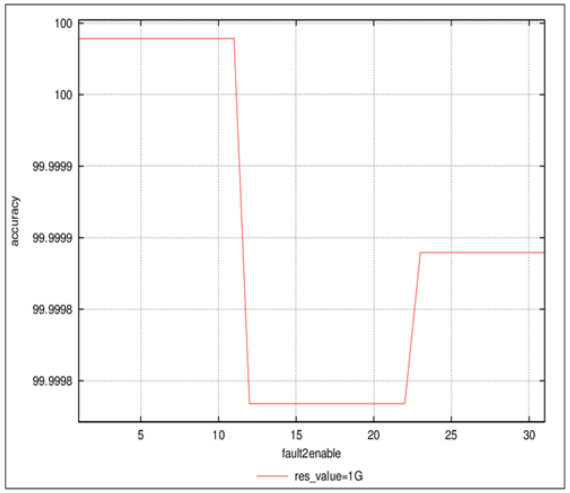
Closed loop system - Experiment Result

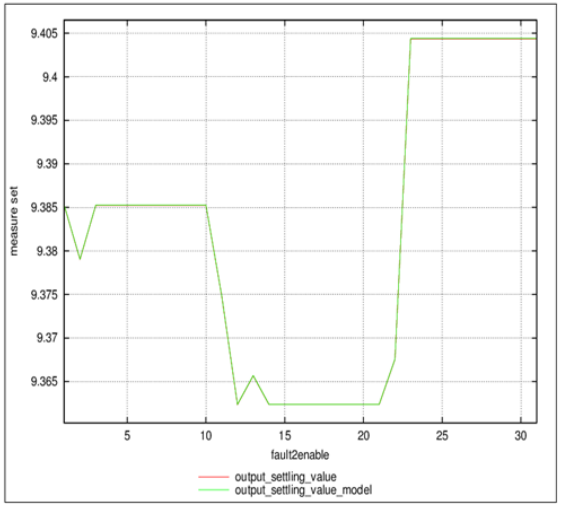


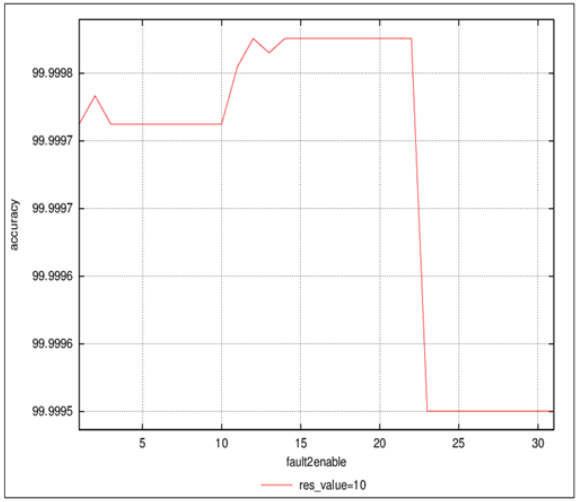
Storage space of Op-Amp
Schematic vs Model

Op-Amp output voltage with faults injected in Bandgap Reference circuit









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