Design & Verification Conference & Exhibition

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Fabric Verification

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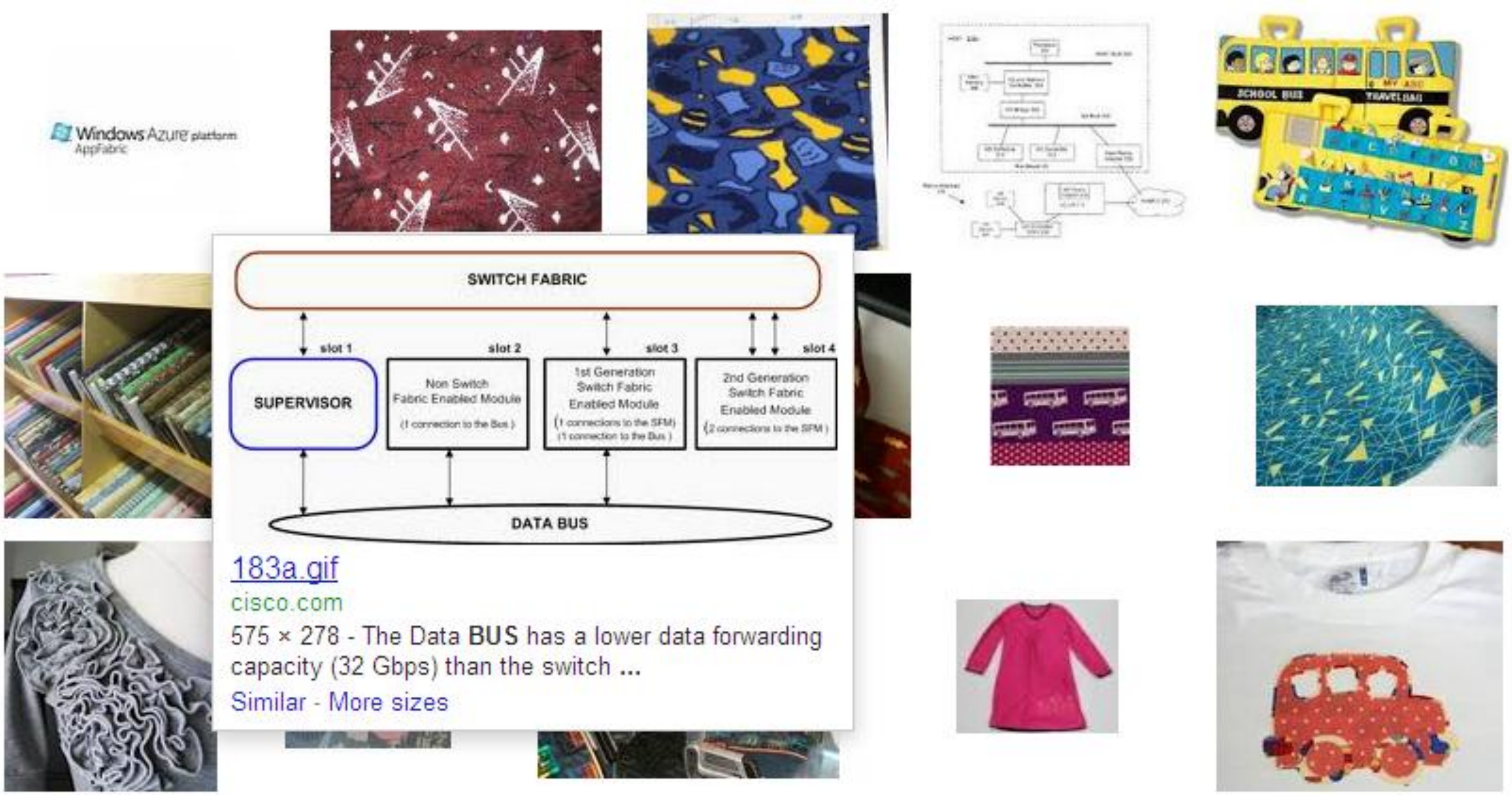
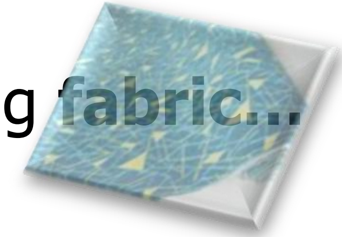
What is a Fabric?

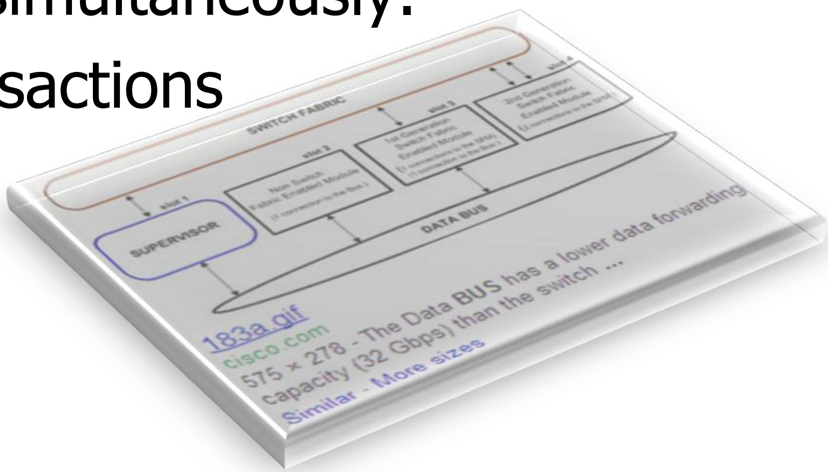


Characteristics of a Bus Fabric

- Resists soda spills and chewing gum – oops wrong fabric...



- Connects multiple masters to multiple slaves.
- Masters can issue transactions simultaneously.
- Masters may issue multiple transactions while earlier transactions are still in flight.
- Some allow transactions to complete out of order.
- Performance impacted by data width and latency.



Verifying a real AMBA3 Switch Fabric

- Basic features must be tested:
  - Check protocol conformance on each port.
  - Check each master can talk to each slave.

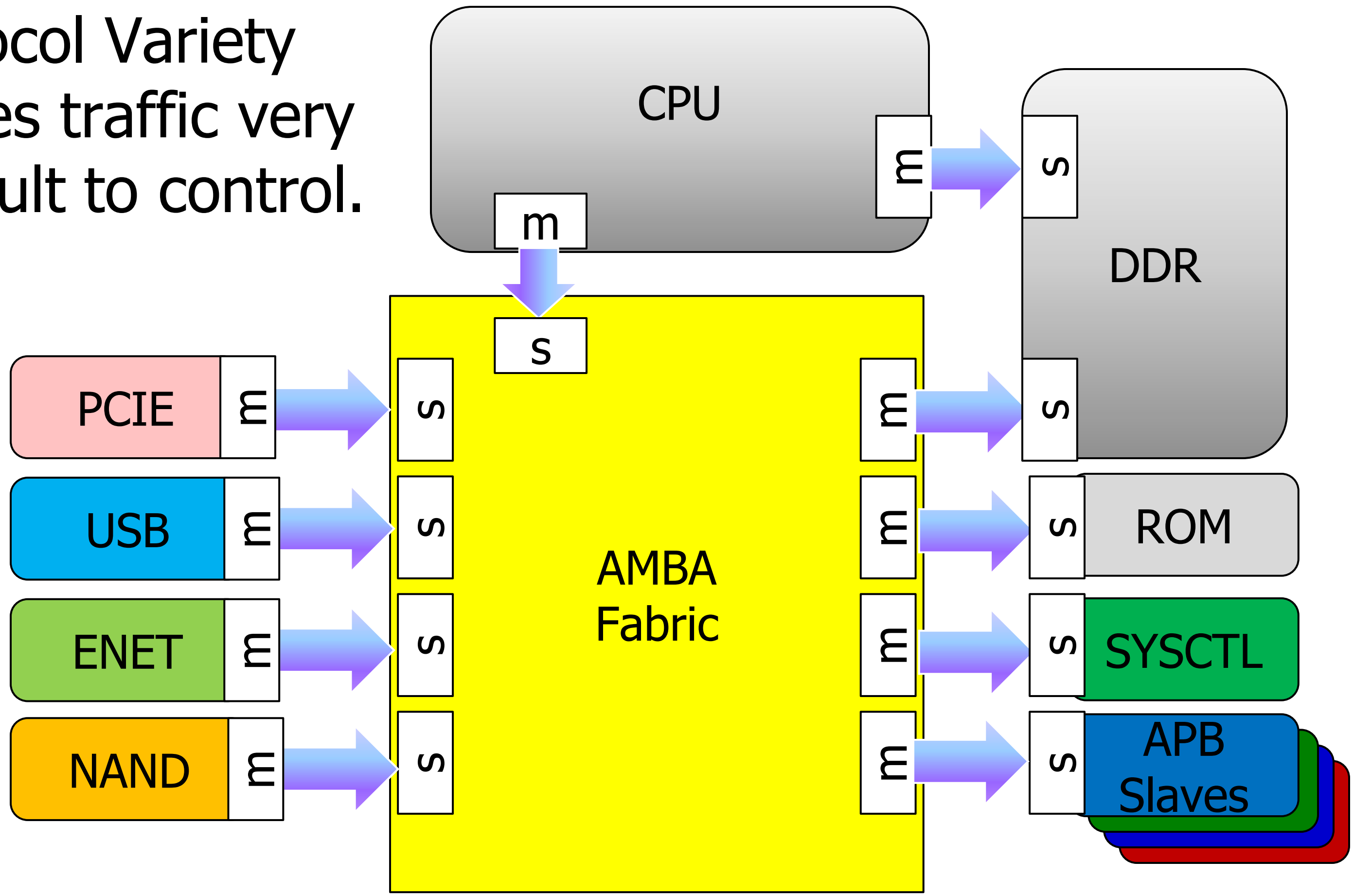
- Basic features aren't enough - these must also be verified:
  - Architectural parameters are correct
  - Bus arbitration on shared segments
  - Conditions that might lead to poor performance
  - Conditions leading to bus stalls or poor latency
  - Performance (bandwidth and latency)

Fabric Verification Goals

- Exhaustive protocol checking
  - Per port, supported features may differ
- Connectivity tests
  - Not a full cross-bar, non-trivial connectivity map
- Arbitration checking
  - Proper algorithms, no starvation scenarios
- Traffic scenario coverage
  - Sparse, Normal, Heavy and variable traffic loads,
- Performance measuring/validation
  - Bandwidth and latency monitoring under all conditions.

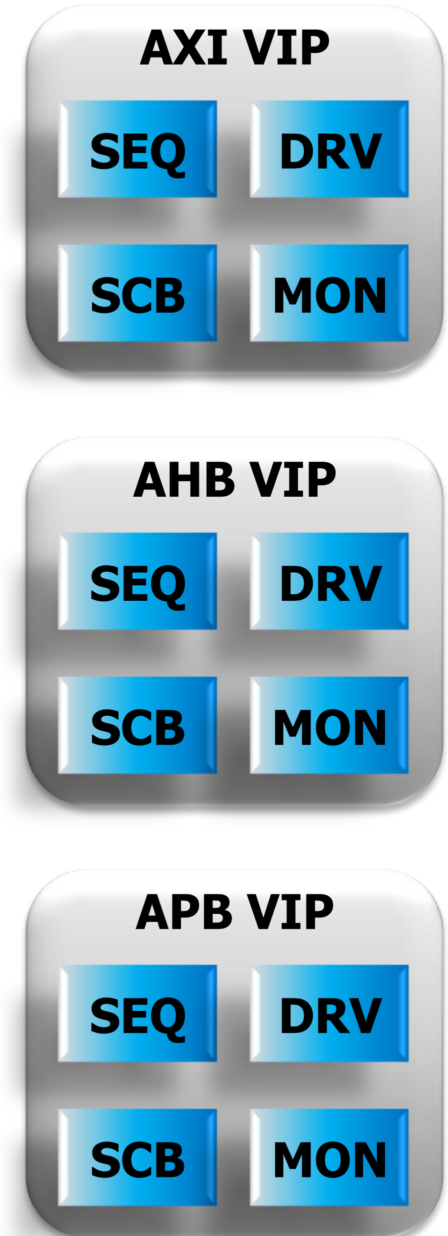
Fabric Topology

- Protocol Variety makes traffic very difficult to control.



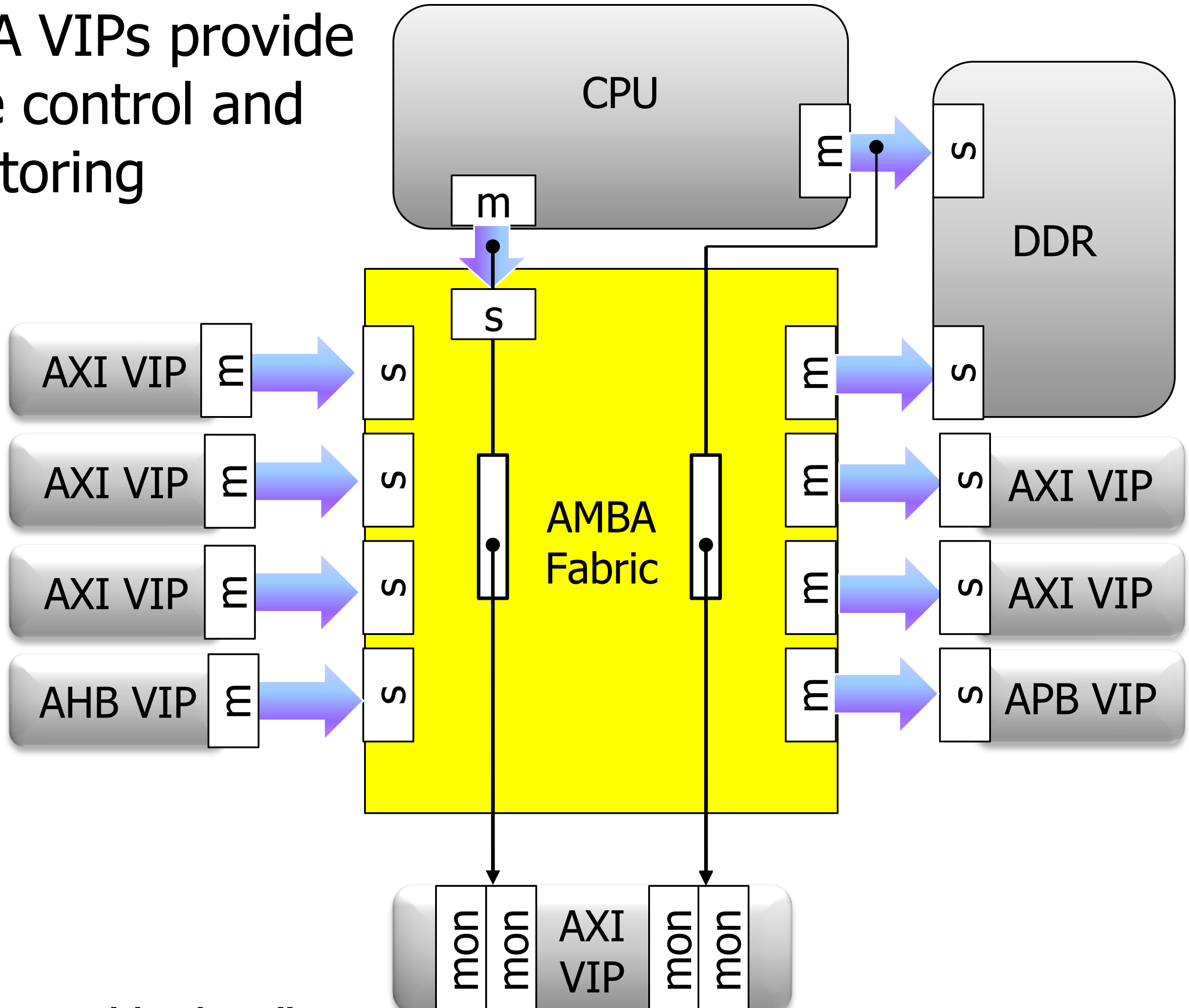
Verification IP

- Will replace peripherals for enhanced controllability and synchronization.
- OVM-native VIP for all AMBA3 protocols (AXI, AHB, APB)
- Protocol monitors, coverage collection, importable test plan
- Support for directed, random, and graph-based sequences
- Compatible with acceleration tools (e.g. Veloce TBX) for really long tests
- Used Questa Verification IP



VIP Connections

- AMBA VIPs provide more control and monitoring



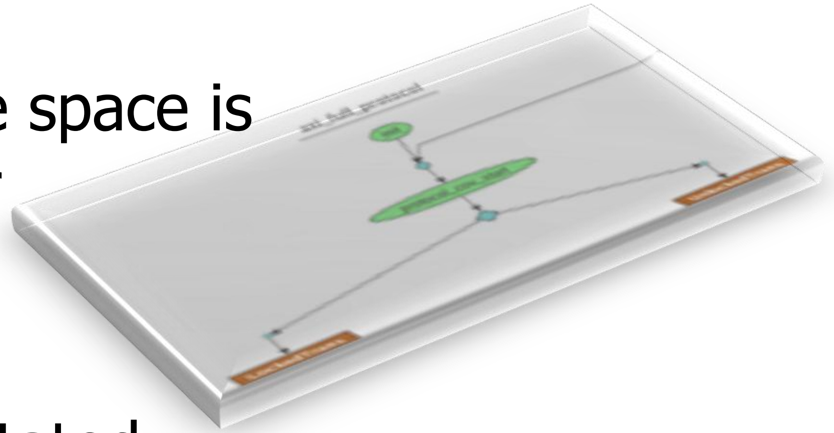
Beyond Constrained Random

- Constrained Random was a leap forward in verification productivity but there are limitations.
- Variables and constraints are sprawling.
- Constraint solvers are proprietary, not consistent.
- Important corner cases are left to chance.
- Coverage models required to determine results.
- If three 7's pay out at 800:1, how many times must the constraint solver "lever" be pulled to cover **777**?

Graph Based Coverage

- Achieves most efficient functional coverage
- No unnecessary repetition
- Provides clear visualization of state space
- Easier definition/review of coverage metrics
- If there are 32 "coverage bins" on this apparatus, cover all of them in 32 "spins".
- Don't gamble with your coverage.

Developing a Graph



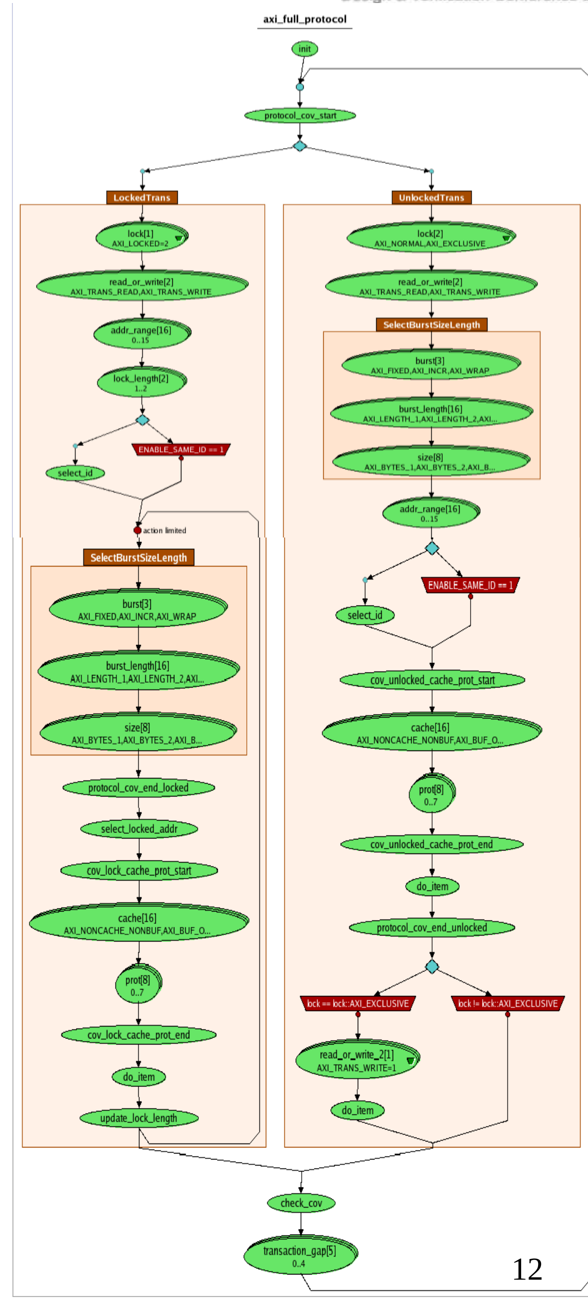
- A particular protocol or coverage space is captured with a simple grammar into a single file.
- It is then compiled into a graph.
- The graph is reviewed and annotated.
- It gives the user strong visual cues about what is covered and what is not covered.
- The annotations inform as to the scale and practicality of the space defined.
- If necessary the user can make informed decisions to limit the scale to a manageable size.
- Alternatively, users can cover full scale large graphs by using coordinated farm servers or acceleration resources.

AXI Rules --> AXI Graph

axi_full_protocol.rules = (~\Local Settings\T... Internet Files\Content.Outlook\IRV77Z6Q) - GVIM

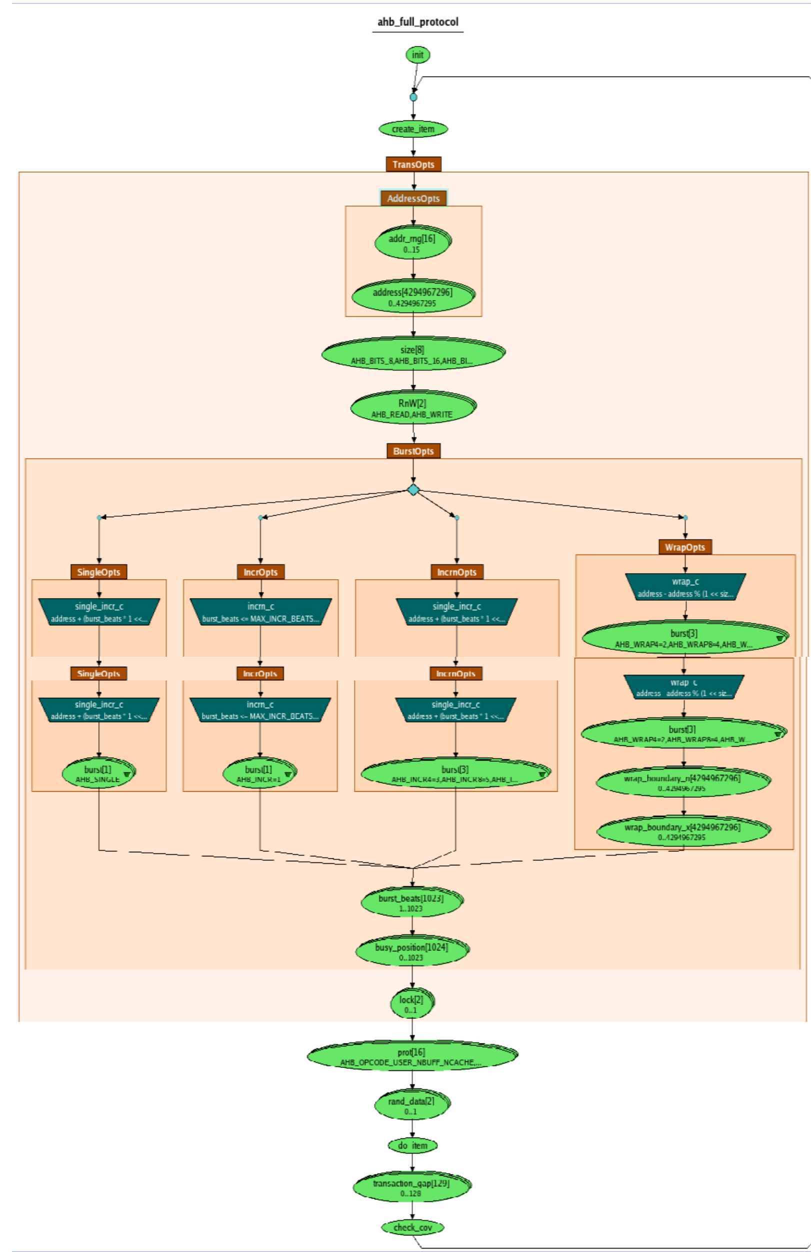
File Edit Tools Syntax Buffers Window Help

```
/*************************************************************************
 *                          axi_full_protocol.rules
 *
 * inFact rules to cover full AXI protocol
 * Copyright 2011 Mentor Graphics Corporation. All Rights Reserved
 *************************************************************************/
rule_graph axi_full_protocol {
    import "infact_axi_param_defs.rseg";
    import "infact_axi_full_protocol_defs.rseg";
    import "infact_axi_full_protocol_burst_controls.rseg";
    // various algebraic constraints omitted for brevity...
    // various symbol definitions omitted for for brevity

    RW_options = (read_or_write[AXI_TRANS_WRITE] rand_data write_strobes) | read_or_write[AXI_TRANS_READ];
    SelectBurstSizeLength = burst
        if {burst == AXI_WRAP} (wrap_boundary_n wrap_boundary_x) | if {burst != AXI_WRAP} eta
        burst_length size;

    UnLockedCacheProtOpts = cov_unlocked_cache_prot_start cache prot cov_unlocked_cache_prot_end ;
    LockedCacheProtOpts   = cov_locked_cache_prot_start cache prot cov_locked_cache_prot_end ;

    UnlockedTrans =
        lock[AXI_NORMAL, AXI_EXCLUSIVE]
        addr_rng address
        select_id | if {EN_SAME_ID == 1} eta

        SelectBurstSizeLength
        // constraint read_or_write_c assures that an exclusive read is selected in RW_options
        RW_options
        UnLockedCacheProtOpts
        do_item
        protocol_cov_end_unlocked
        if {lock == AXI_EXCLUSIVE} (
            excl_transaction_gap // let excl read trans register with QVL monitors
            read_or_write_2[AXI_TRANS_WRITE] // exclusive access must be ended with a write
            rand_data write_strobes
            do_item
        ) | if {lock != AXI_EXCLUSIVE} eta ;

    LockedTrans =
        lock[AXI_LOCKED]
        addr_rng
        select_id | if {EN_SAME_ID == 1} eta
        lock_length
        repeat action_limited {
            SelectBurstSizeLength
            RW_options address
            protocol_cov_end_locked
            LockedCacheProtOpts
            do_item
            update_lock_length
            lock_transaction_gap };

    // TOP of graph
    axi_full_protocol = init repeat {
        external_sync
        create_item
        protocol_cov_start
        LockedTrans | UnlockedTrans
        check_cov
        transaction_gap };
}
~
                                                          22,1          All
```



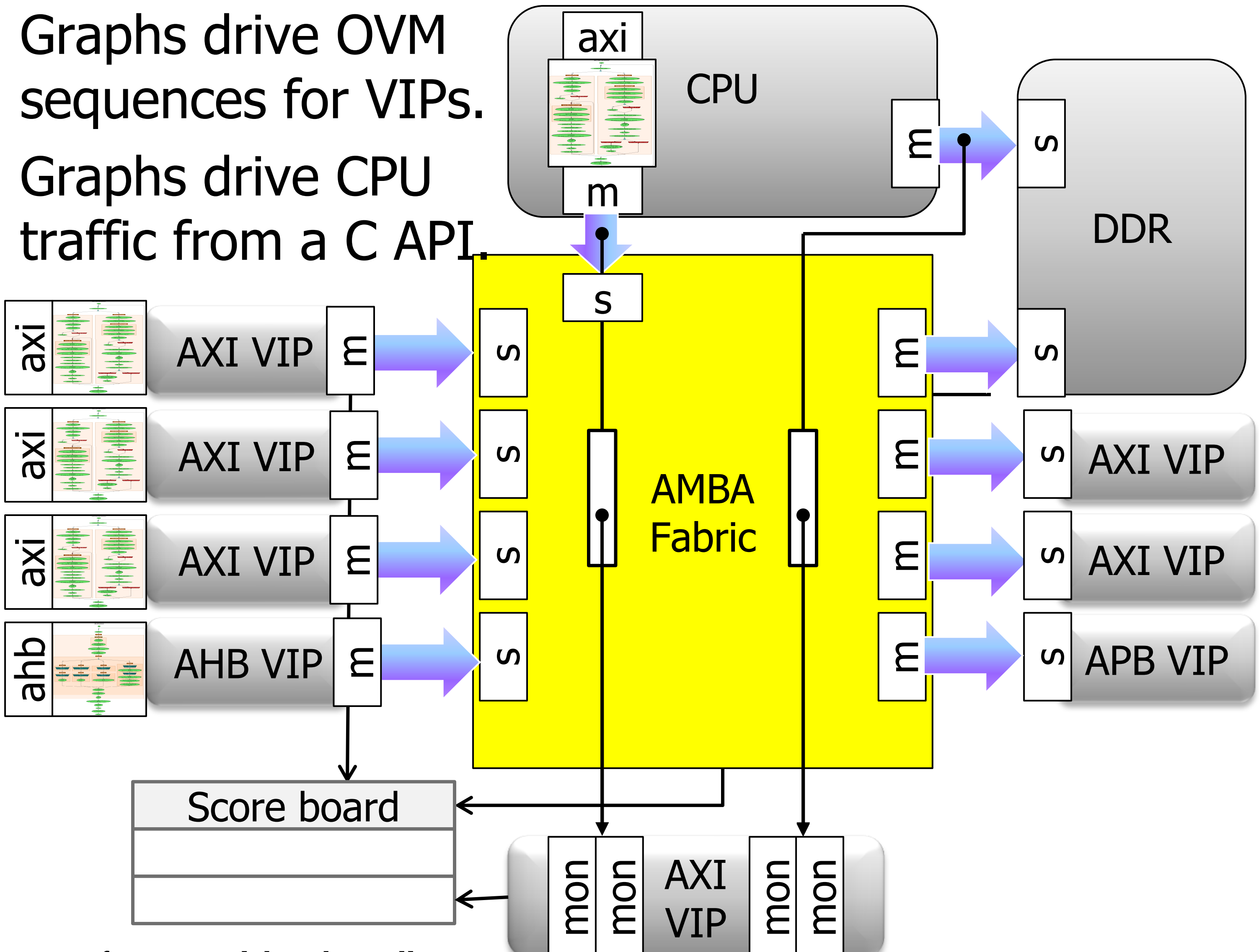
AHB Graph

- These graphs will cover the full spectrum of their respective protocols.
- Full protocol compliance is covered efficiently in a few hundred thousand clock cycles.
- Graphs can stop or continue looping to cover more address or data ranges generating long streams of useful bus traffic.



Graph-based Sequences & API

- Graphs drive OVM sequences for VIPs.
- Graphs drive CPU traffic from a C API.



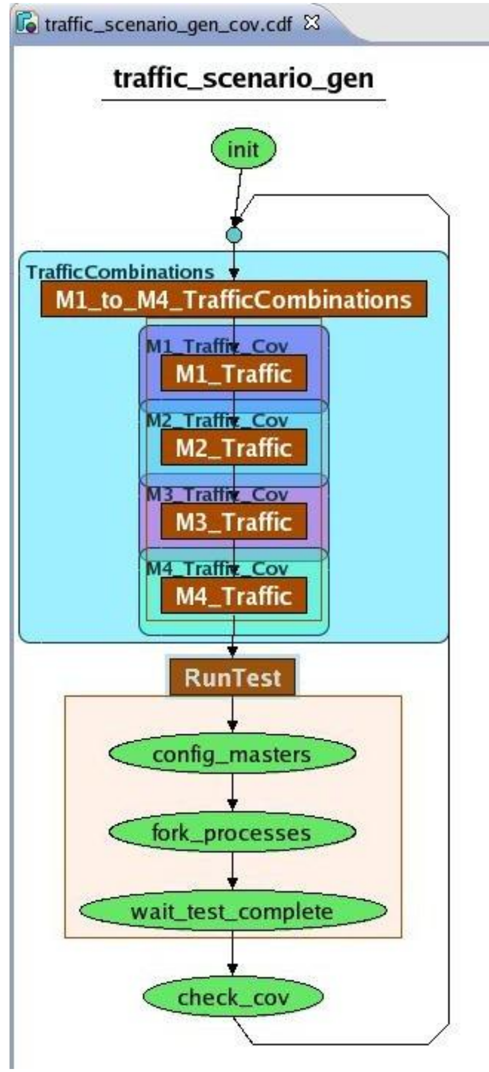
Traffic Control and Modulation

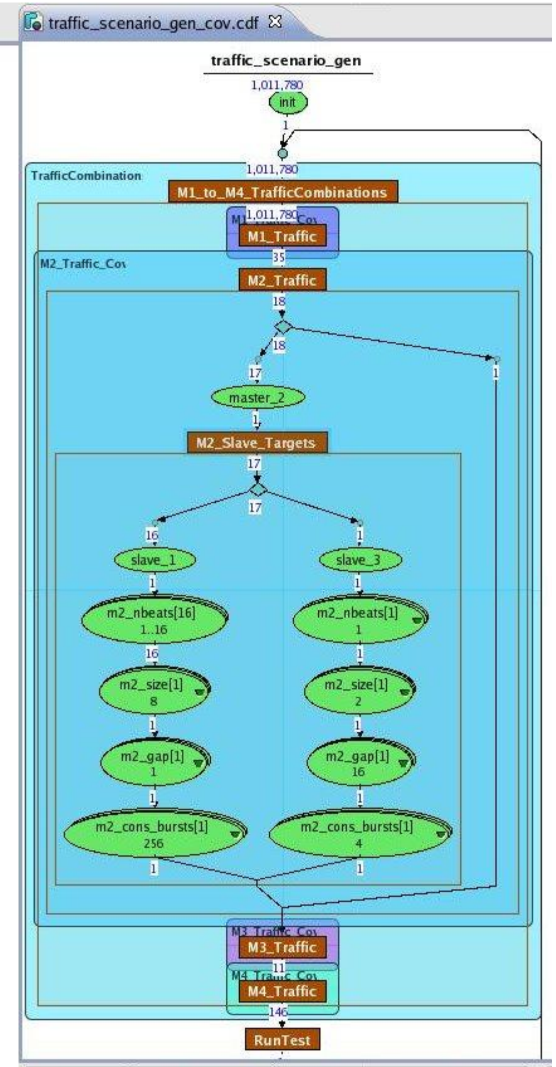
- The goals are to first operate the fabric under normal and expected traffic conditions.
- Next, we want to put the fabric under as
- many conditions of duress as possible.
- We need to determine if there are any sets of traffic conditions that cause the fabric to:
  - Slow down to unacceptable performance
  - Block out certain masters or slaves
  - Lock up the system.

- Traffic modulation allows us to shape the traffic into scenarios that match light, normal or heavy traffic patterns.

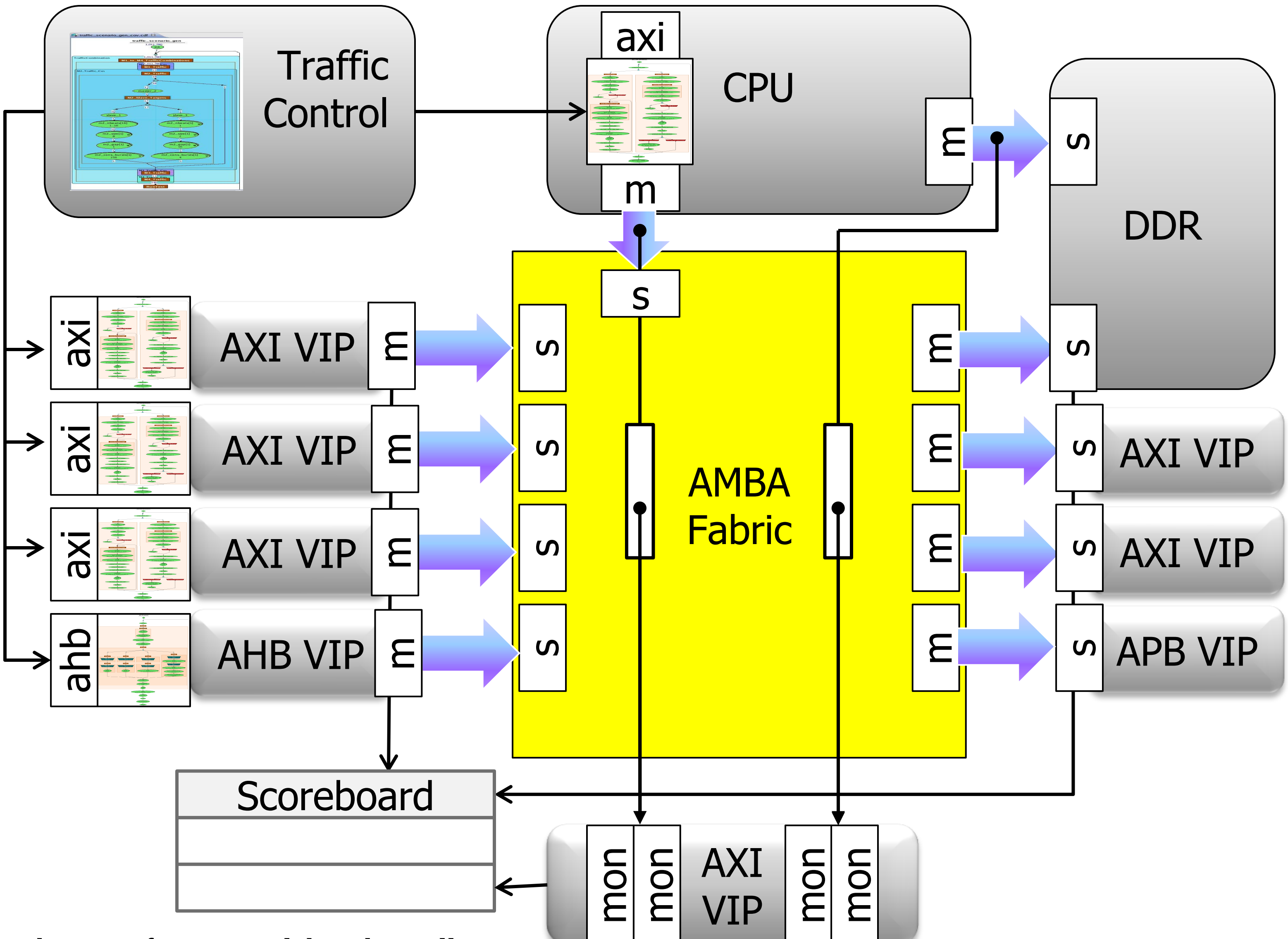
Traffic Coordinating Graph

- Each protocol graph can be controlled by the traffic control graph.
- The traffic control graph can continuously adjust settings for each master to modulate local traffic.
- The traffic control graph can take over and precisely control the local graph giving it the ability to synchronize traffic on each master.



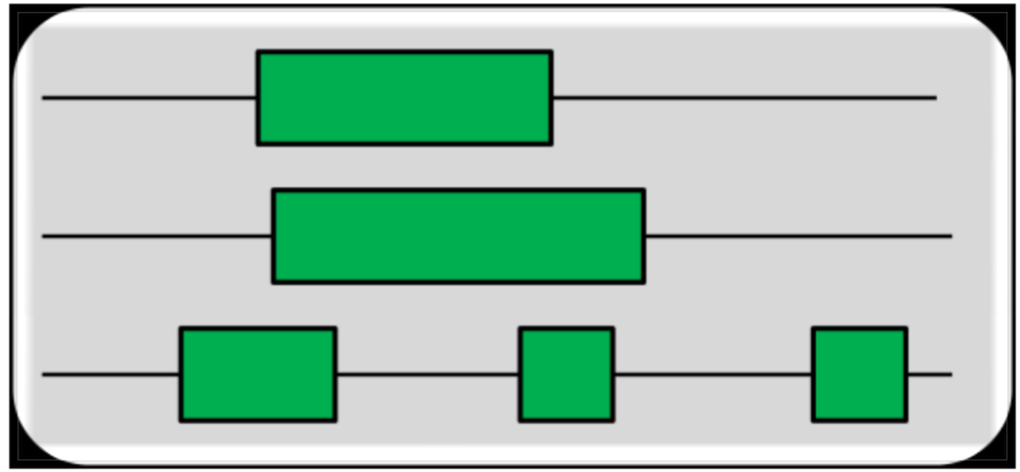


Traffic Control and Modulation

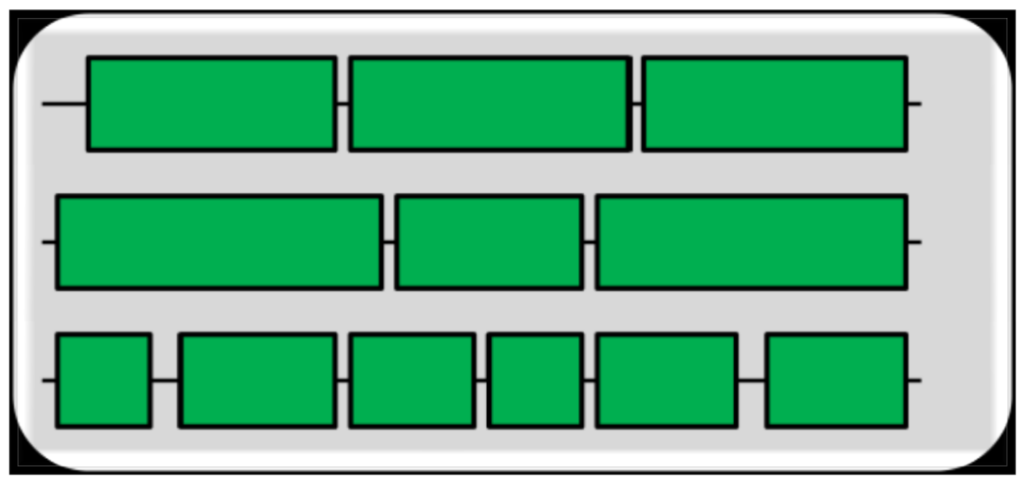


Traffic Scenarios

- This diagram shows a normal traffic scenario.
- Bus activity is dense during a buffer transfer.
- Bus activity goes quiet while waiting new for transfers to start.



- This diagram shows a heavy traffic scenario.
- There is very little quiet time between large transfers.



Traffic Control Scenarios

- The traffic control graph allows us to target specific features and performance of the fabric as a fabric instead of treating it as an array of ports.

Conclusion

- We have already proven the effectiveness of several components of this solution resulting in improved designs and schedules.

- As we scale up the small traffic control example shown here to the full chip level we expect continued design improvements and confidence.